Gate tunable graphene-silicon Ohmic/Schottky contacts

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We show that the *I-V* characteristics of graphene-silicon junctions can be actively tuned from rectifying to Ohmic behavior by electrostatically doping the graphene with a polymer electrolyte gate. Under zero applied gate voltage, we observe rectifying *I-V* characteristics, demonstrating the formation of a Schottky junction at the graphene-silicon interface. Through appropriate gating, the Fermi energy of the graphene can be varied to match the conduction or valence band of silicon, thus forming Ohmic contacts with both *n*- and *p*-type silicon. Over the applied gate voltage range, the low bias conductance can be varied by more than three orders of magnitude. By varying the top gate voltage from −4 to +4 V, the Fermi energy of the graphene is shifted between −3.78 and −5.47 eV; a shift of ±0.85 eV from the charge neutrality point. Since the conduction and valence bands of the underlying silicon substrate lie within this range, at −4.01 and −5.13 eV, the Schottky barrier height and depletion width can be decreased to zero for both *n*- and *p*-type silicon under the appropriate top gating conditions. *I-V* characteristics taken under illumination show that the photo-induced current can be increased or decreased based on the graphene-silicon work function difference. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4768921]

Metal-semiconductor interfaces form Schottky junctions due to the mismatch of their work functions and electron affinities.[1] These junctions are characterized by a Schottky barrier, a depletion width, and a rectifying behavior. In typical MOSFET devices, regions of heavily doped semiconductor are needed in order to reduce the high resistance associated with these metal-semiconductor junctions. However, these p^+ and n^+ regions present several problems as the channel lengths of transistors are scaled down to the 22 nm node and beyond. For example, diffusion of dopants into the active channel region can cause a significant reduction in the gain of these devices. Therefore, a method for producing low (or zero) Schottky barrier metal-semiconductor junctions without doping the semiconductor is highly desirable.

Polymer electrolyte doping has been reported as an effective way of doping carbon nanotubes and graphene.[2–5] Lu *et al*. fabricated polymer electrolyte-gated carbon nanotube transistors,[6] and Das *et al*. reported electrochemical top-gated graphene transistors, which show that the Fermi energy of graphene can be shifted by over 0.7 eV.[7] From these previous works, the Fermi energy of graphene in our experiment is estimated to be shifted by ±0.85 eV from the charge neutrality point by polymer electrolyte doping.

In our previous work, Schottky diode behavior was demonstrated in graphene-silicon junctions using a simple fabrication technique.[8] Tongay *et al*. have observed Schottky contacts between bulk graphite and Si, GaAs, 4H-SiC, and GaN substrates.[9,10] In these previous works, however, the Fermi energy of the graphene was not varied by an external gate. The Schottky junction behavior at graphene-semiconductor interfaces and graphene's highly transparent nature have also been extended to photovoltaic applications.[11–15] Graphene-silicon nanowire Schottky junctions have reported solar conversion efficiencies of 1.25%. The conversion efficiency of these graphene-silicon devices could be further improved by exposing the graphene to $SOCl_2$ and HNO_3 vapors, which leads to *p*-type doping of the graphene.[16,17] In this prior work, the enhancement in energy conversion efficiency was attributed to the increased graphene conductance caused by *p*-type doping. However, it is also likely that the variation of the Schottky junction with doping also contributed to their experimental observations. Tongay *et al*. have studied the effect of bromine intercalation of graphite on the Schottky barrier height formed at many-layer-graphene (MLG)/GaN interfaces.[10,18] These previous works suggest that the electron transport in these devices can be changed by shifting of the graphene work function.

In this paper, we measure the *I-V* characteristics of graphene-silicon contacts while varying the work function (i.e., Fermi energy) of graphene. We explore the effects of both *n*- and *p*-type doping of graphene on the conductance of the interface, for both *n*- and *p*-type silicon substrates. Photocurrent generation in these graphene-silicon junctions is also studied as a function of graphene doping, in order to further understand the Schottky/Ohmic nature of the junction.

Graphene is grown on copper foil by chemical vapor deposition (CVD).[19–24] Poly(methyl methacrylate) (PMMA) is then spin coated on the graphene surface right after the growth to avoid unwanted doping from air and to prevent the graphene film from breaking during the graphene transfer process. The underlying copper foil is then etched away using copper etchant to separate the graphene film from the copper foil. Before transferring the graphene film, an oxidized silicon wafer is patterned photolithographically to expose 300 × 300 μm windows, which are subsequently etched using buffered oxide etch (BOE) 7:1 in order to remove the SiO_2 and expose the underlying silicon. Pd/Ti (50/5 nm thickness) electrodes are deposited 100 μm away from the silicon windows, as shown in Figure 1(a). Graphene films are then transferred to the prepared substrates, and the

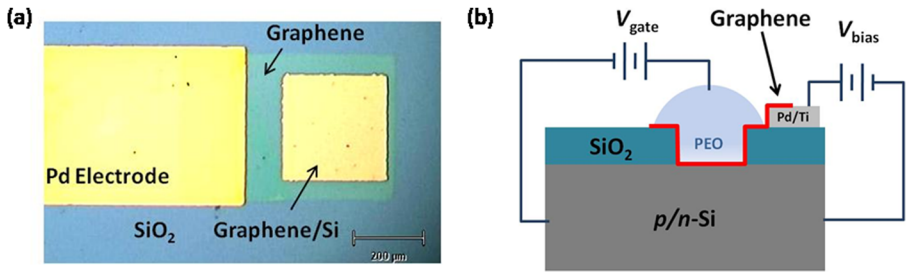

FIG. 1. (a) Optical microscope image of the graphene-on-silicon device before depositing the electrolyte top gate and (b) schematic diagram of the device structure.

PMMA is removed by acetone vapor. Another photolithography step is performed to etch all of the graphene in between adjacent devices. The polymer electrolyte is prepared by dissolving poly (ethylene oxide) (PEO) and lithium perchlorate ($LiClO_4$) (1:0.12 by weight) in methanol.[6] It is then applied locally to the graphene-silicon contact region of the device, as shown schematically in Figure 1(b). A small bias voltage is applied between the graphene (through the Pd electrode) and the underlying silicon substrate. The top gate voltage is applied by inserting a small probe into the polymer.

Figure 2(a) shows the I-V_{bias} characteristics taken at various top gate voltages ranging from -4 V to $+4$ V for a p-type silicon wafer (100 Ω/cm, $p \sim 1.25 \times 10^{14}\,cm^{-3}$). The inset figure shows the I-V_{bias} characteristics of the device taken at zero gate voltage, which exhibits rectifying behavior, indicating the formation of a Schottky junction. As a large negative (p-doping) gate voltage is applied, the I-V_{bias} characteristics evolve to Ohmic behavior, indicating a reduction of the Schottky barrier height and depletion width. Figure 2(b) shows the I-V_{bias} characteristics of a graphene-silicon interface for an n-type silicon wafer (15 Ω/cm, $n \sim 2.5 \times 10^{14}\,cm^{-3}$). In this dataset, the opposite behavior is observed, in which Ohmic behavior appears at large positive (n-doping) gate voltages.

Figures 3(a) and 3(b) show the low bias conductance plotted as a function of the Fermi energy of graphene for p- and n-type silicon substrates, respectively. Over the applied gate voltage range, the conductance is varied by more than three orders of magnitude. The charge neutrality point was determined from the I-V characteristics of a similar graphene sample with source and drain electrodes in a field-effect transistor geometry.[25,26] The device geometry and experimental results are shown in the supplemental document as Figures S1(a) and S1(b).[27] These data indicate that the charge neutrality points occur at $V_g = 0.19$ V and 0.20 V, respectively, for graphene on p- and n-type silicon substrates. The graphene Fermi energy ($E_F^{graphene}$) is determined from the applied gate voltage using a top gate capacitance of 2.2×10^{-6} F/cm^2, as described by Das *et al.*[7] In Figure 3, the work function of graphene is shifted between -3.78 and -5.47 eV, which corresponds to $+0.82$ and -0.87 eV from the charge neutrality point.[28,29] The conductance data in Figure 3 were collected under low bias voltages ranging from -0.02 V to 0.02 V, which should have a negligible effect on the doping of the graphene. Therefore, the graphene Fermi levels under various gate voltages are considered the same as those obtained from the transistor measurement. The solid vertical lines in the plots correspond to the conduction (E_c^{Si}) and valance (E_v^{Si}) bands of silicon, and the dashed line indicates the Fermi energy of the silicon substrate (E_F^{Si}). For the p-type silicon sample (Figure 3(a)), the low bias conductance increases as the graphene Fermi energy is decreased and tends to saturate after passing the valence band of silicon. For the n-type sample (Figure 3(b)), the conductance increases as the graphene Fermi energy approaches the conduction band of silicon. These observations indicate that p-type (n-type) doping of graphene leads to a decrease of the Schottky barrier formed with the underlying p-type (n-type) silicon, thus, leading to a transition from rectifying to Ohmic behavior, as observed in Figure 2.

Figure 4(a) shows the graphene-silicon I-V_{bias} characteristics for a p-type silicon substrate taken at different gate voltages under illumination with a 50 W fiber optic illuminator. For large negative gate voltages, we observe Ohmic behavior with no photo-generated current or voltage. Figure 4(b) shows the short circuit current (I_{sc}) dependence on the graphene Fermi energy, which increases sharply when the Fermi energy of the graphene exceeds that of the silicon substrate,

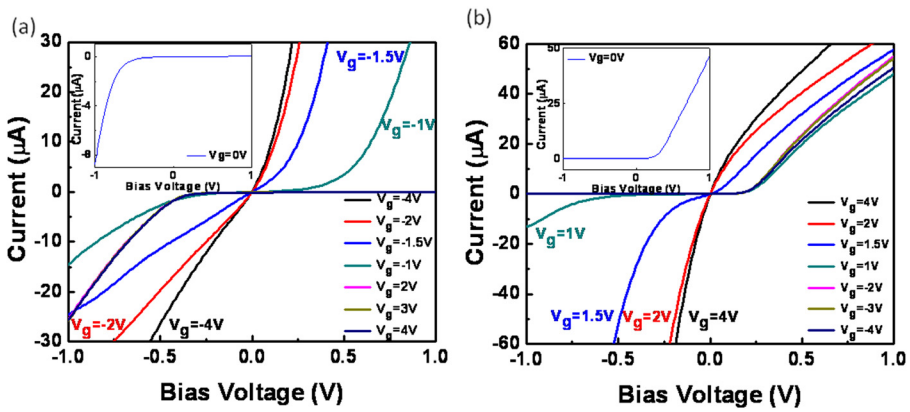

FIG. 2. I-V_{bias} characteristics taken at different gate voltages (V_g) of (a) graphene-Si (p-type) and (b) graphene-Si (n-type) devices. The inset figures show the I-V characteristics at $V_g = 0$ V.

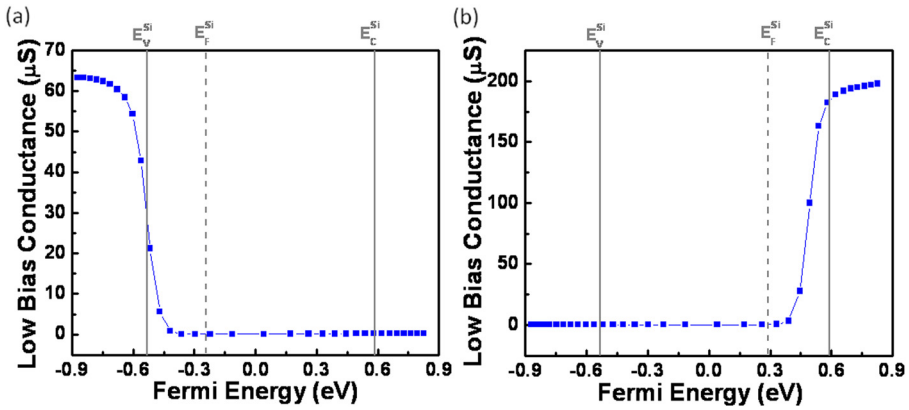

FIG. 3. Low bias conductance plotted as a function of graphene Fermi energy for (a) graphene-Si (*p*-type) and (b) graphene-Si (*n*-type) devices. The right and left solid vertical lines represent the conduction and valence bands of silicon, and the middle dashed line represents the Fermi energy of silicon.

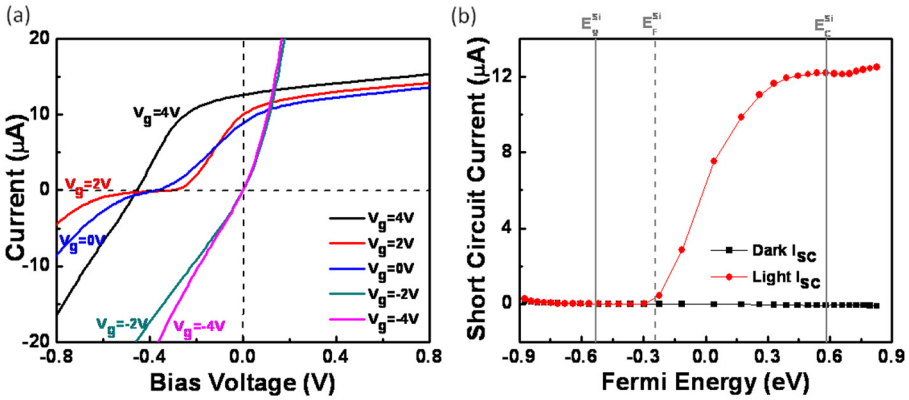

FIG. 4. (a) Graphene-silicon I-V_{bias} characteristics taken under illumination at different gate voltages. (b) Short circuit current (I_{sc}) with and without illumination plotted as a function of graphene Fermi energy.

and then saturates in the region near the conduction band of silicon. This implies that the depletion region in the underlying silicon substrate increases with the electron carrier concentration in the graphene. The increased depletion region is able to collect more light, thus resulting in an increased photocurrent. As mentioned above, Fan *et al.* also observed I_{sc} enhancement in their graphene-silicon device with chemical vapor doping, and attributed the I_{sc} enhancement to the increase in graphene conductance.[16] However, both *p*- and *n*-type doping cause an increase in graphene conductance. Therefore, the increased depletion width provides a more plausible explanation of the I_{sc} enhancement with graphene doping.

Since the graphene is two-dimensional, it does not completely screen the gate field, which will penetrate into the Si, resulting in modulation of carrier concentrations in Si.[30] We, therefore, must consider depletion and/or accumulation of the Si substrate in our analysis. First, the Schottky barrier height is independent of silicon doping, and only depends on $E_c^{Si} - E_F^{graphene}$ for *n*-type silicon and $E_F^{graphene} - E_v^{Si}$ for *p*-type silicon. So, to first order, we do not expect the gate doping of the silicon to play a significant role in the *I*-*V* characteristics. Furthermore, since the graphene and silicon are either both *n*-doped or both *p*-doped, the effect of the gate on silicon will not switch between rectifying and Ohmic behavior. Also, since the density of states of the silicon is much larger than that of the graphene, we expect the relative change due to the gate to be negligible compared with graphene (i.e., $\Delta E_F^{Si} \ll \Delta E_F^{graphene}$). Finally, from Figure 4(b), the short circuit photocurrent generation is not observed until the Fermi energy of graphene meets that of the silicon, where the depletion region begins to build. This experimental observation is consistent with the theoretical estimation of the graphene Fermi energy, and provides further evidence that the effects of gate doping in the underlying silicon substrate are negligible.

In conclusion, the *I*-*V* characteristics of graphene-silicon contacts can be tuned from rectifying to Ohmic behavior by electrostatically doping the graphene with a polymer electrolyte gate. We explore the effects of both *n*- and *p*-type doping of graphene on the *I*-*V* characteristics of the interface, for both *n*- and *p*-type silicon substrates. Through appropriate gating, the Fermi energy of the graphene can be varied to match the conduction or valence band of silicon, thus forming Ohmic contacts with both *n*- and *p*-type silicon. Similarly, the Schottky barrier height and depletion width can also be increased with electrostatic gating, resulting in rectifying diode behavior and large photocurrents. Over the applied gate voltage range, the low bias conductance can be varied by more than three orders of magnitude.

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