RF receiver with integrated blind-source separation

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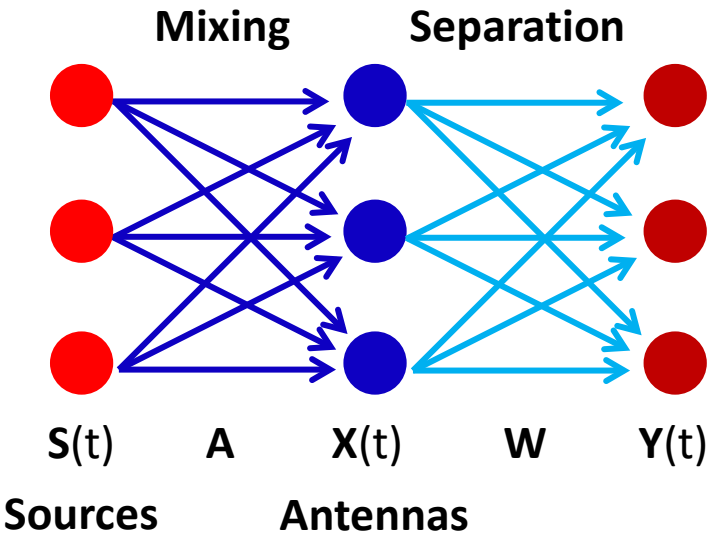
Motivation: The cocktail party problem

- Suppose there are simultaneous independent conversations at a cocktail party and, without prior knowledge of individual voices or languages, your objective is to isolate each speaker (or source)
  - This is a blind-source separation problem
- Using multiple microphones, the linearity of the system, and the fact real-time audio signals are independent and not Gaussian noise, it is possible to use independent component analysis (ICA) or machine learning (ML) to solve the inverse problem
  - This is an *inverse problem* (a subset of more general optimization) because the (solution) sources are known to exist

Motivation: Applying the cocktail party problem to RF signals



- In the RF environment the equivalent of multiple voices at a cocktail party are unknown sources of complex signals (they have I and Q components) with frequency, temporal, and spatial characteristics
  - Blind-source separation (followed by classification and demodulation) of signals is of interest in both commercial (e.g. cognitive radio) and military (e.g. urban environment) applications
- The linear *N*x*N* mixing matrix **A** gives complex RF input at the *N* antennas

  $\mathbf{X}(t) = \mathbf{A}\mathbf{S}(t)$

  Only the measured signals **X** at each antenna are known. The mixing matrix **A** and the source signals **S** are unknown. The objective is to find the unknown original complex signals

  $\mathbf{S}(t) = \mathbf{A}^{-1}\mathbf{X}(t)$

  If $\mathbf{A}^{-1}$ exists then ICA can find an approximation of $\mathbf{A}^{-1}$ and unmix the linear combination to give

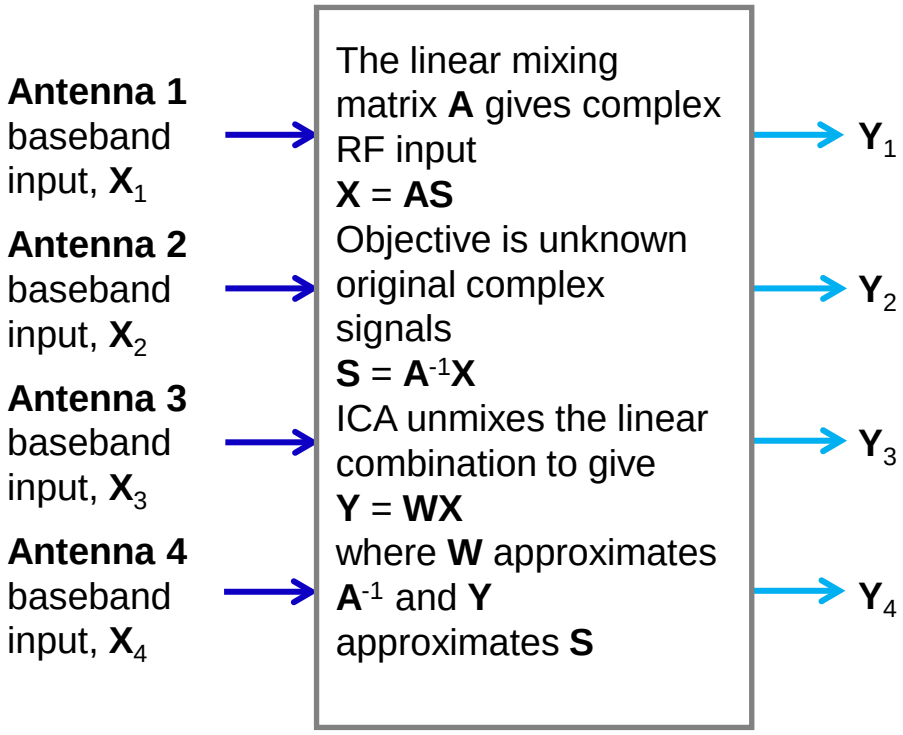
  $\mathbf{Y}(t) = \mathbf{W}\mathbf{X}(t)$

  where **W** approximates $\mathbf{A}^{-1}$ and **Y**(t) approximates **S**(t)

Motivation: Blind-source separation of multiple signals using ICA chip *before* digitization in RF receiver

- ICA can separate *N*-signals from an *N*-antenna receiver
  - It is also possible to separate more than N signals
- Because ICA signal separation can be performed in a mixed-signal circuit ***before digitization***, the ADC requirements of the receiver can be relaxed
- The ICA signal separation function implemented in hardware before digitization *off-loads* receiver DSP requirements
- The mixed-signal circuit performs efficient matrix multiplication **Y** = **WX** via programmable multiply–accumulate operations (MAC) on real-time complex signals
  - Because programmable matrix multiplication is a general operation, it can be used to perform *other* signal processing functions prior to digitization

ICA chip performs blind-source signal separation before RF receiver ADC

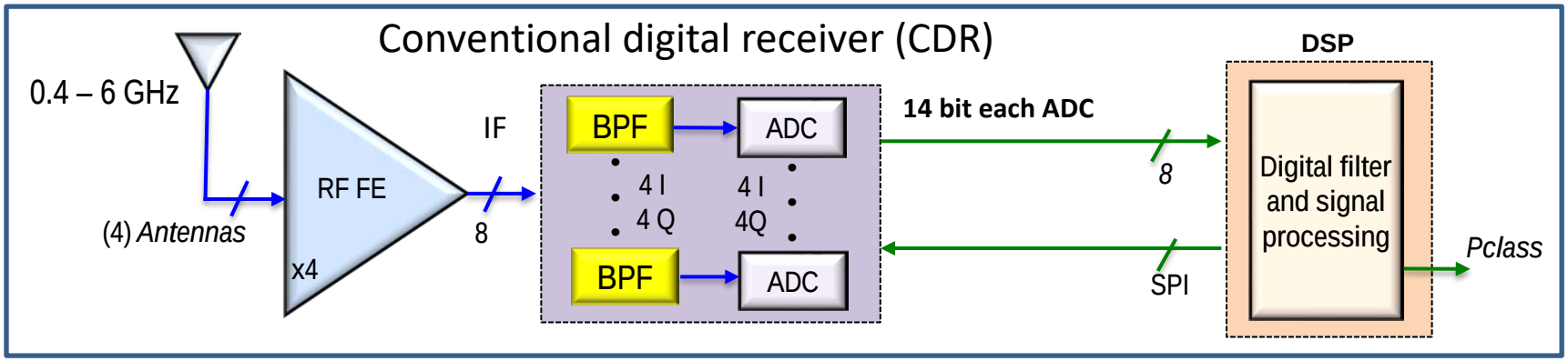


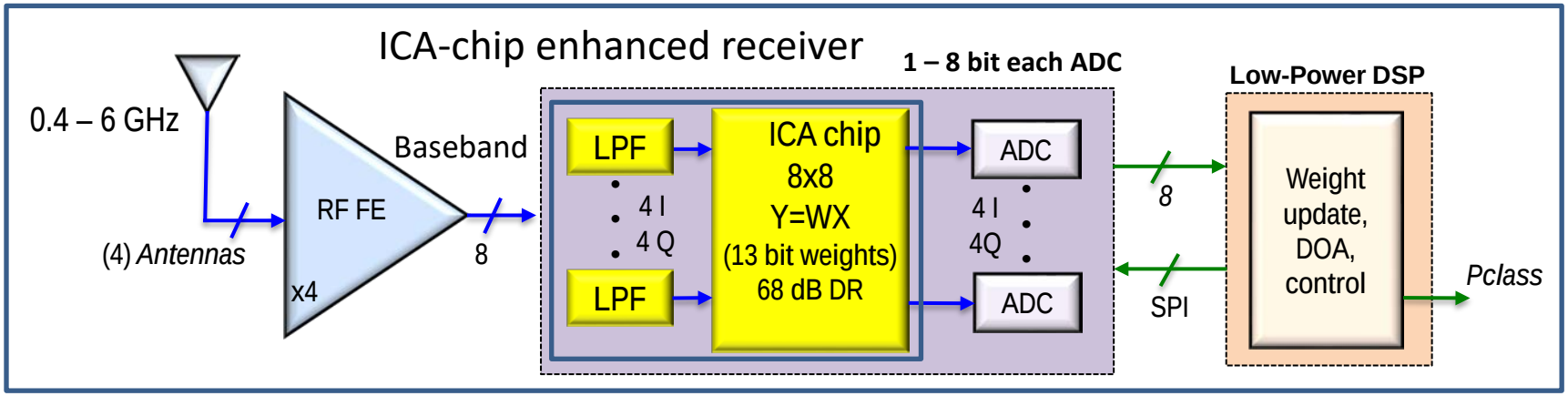
Analog signals **Y** characterized by correlation to **S** using coefficient

$C_{xy}=|\mathbf{S}_x^T \cdot \mathbf{Y}_y|$

Conventional digital receiver versus ICA-chip enhanced receiver

- **Conventional digital receivers are susceptible to jammer interference in EW and cognitive radio**
- **Fundamental to conventional digital receiver is that the SUM of all received signals MUST be digitized first** because any DSP processing and **blocking of jammer signal can only occur AFTER the ADC**
  - Full burden on ADC and DSP
- **The ICA chip can spatially block jammers BEFORE the ADC and this allows relaxed ADC specification** (e.g. 2-3 bits of linearity required for convergence of matrix weights, 8 bits for demodulation, etc.)
  - Adaptive offload of ADC and DSP



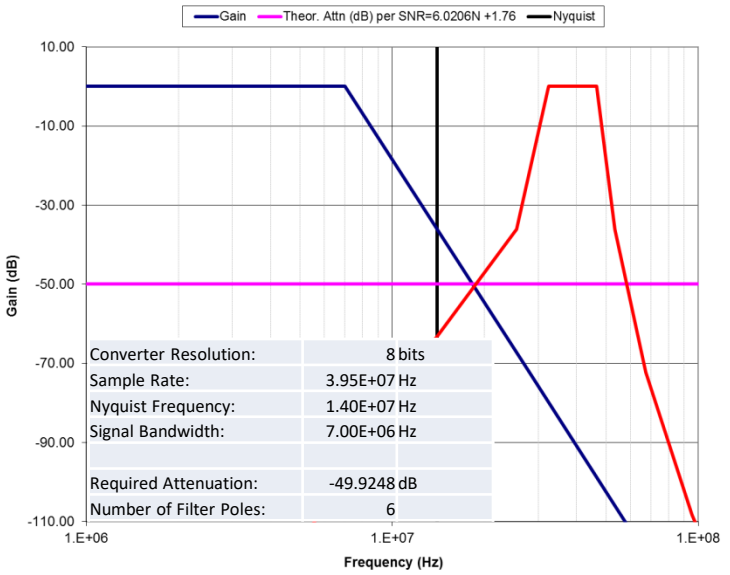


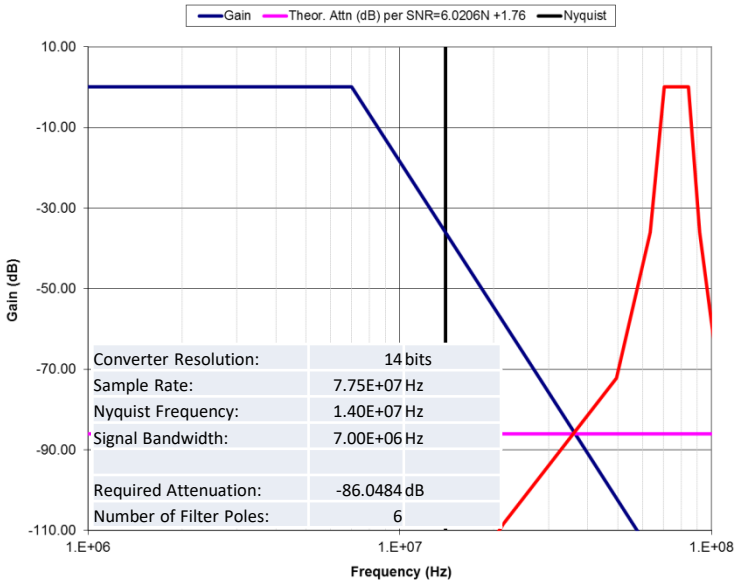
Conventional digital receiver versus ICA-chip enhanced receiver

- Typically, max. 1Vpp limited by VDD=1.2V, 62dB DR (10-b), 20dB SNR (0.1mVpp) -> +4-b digital receiver
- For fixed bandwidth and fixed number of poles in anti-alias filter, the extra bits of resolution required in digital receiver increases sampling rate to protect against aliasing

EXAMPLE

- BW=7MHz (Nyquist sampling rate is 14MS/s) and 6-pole anti-alias filter (attenuation -120dB/decade)
  - For N-bit ADC sampling at rate f_S, filter attenuation must be below SNR at frequency $f_S/2$
  - $f_S=2xBWx10^{SNR(dB)/(\#polesx20dB)}$
  - SNR=(Nx6.0206+1.761)dB
- ICA chip with 3-b ADC (SNR=20dB) to converge algorithm matrix weights samples at 22MS/s (1.6xNyquist)
- ICA chip with 8-b ADC (SNR=50dB) to demodulate samples at 40MS/s (2.8xNyquist)
- Conventional digital receiver with 14-b (SNR=86dB) ADC samples at near 80MS/s (5.7xNyquist)

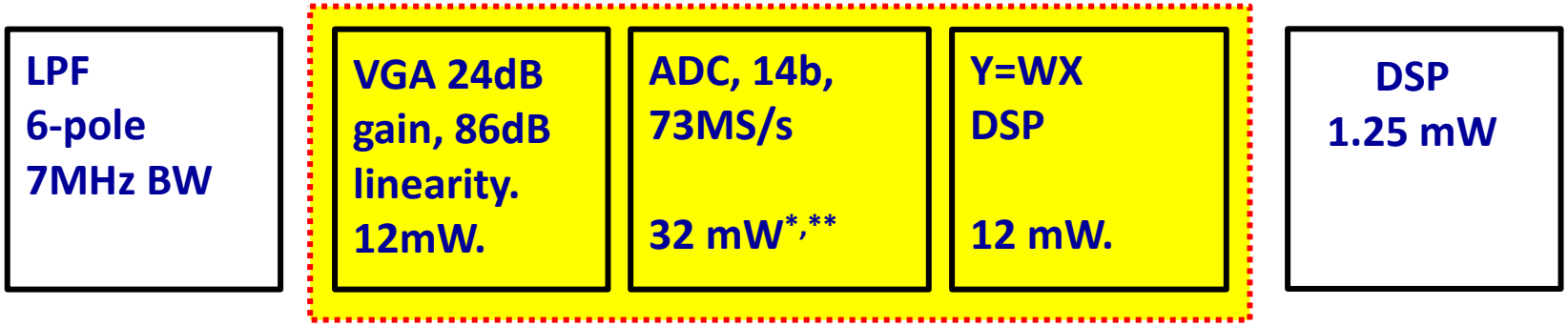




Conventional digital receiver versus ICA chip (single channel)

Current ICA chip in 65nm CMOS
10mW/channel (current spin/design time) or <1mW/channel with additional design time.
Use 1mW/channel for comparison of *potential* power savings versus CDR

CDR replicating current ICA chip in 65nm CMOS consumes 12+32+12=56 mW/channel.
DSP 73MS/s*16*10pJ/OP=11.68 mW.



*Analog Devices AD9269 = 44mW Power Dissipation at 20 MSPS/Channel (36 fJ/conversion)
**Analog Devices research 14b, 80MS/s, 35.1mW (with ref) in 65nm CMOS, ISSCC 2013 (26 fJ/conversion) ^ TMSC320C5534

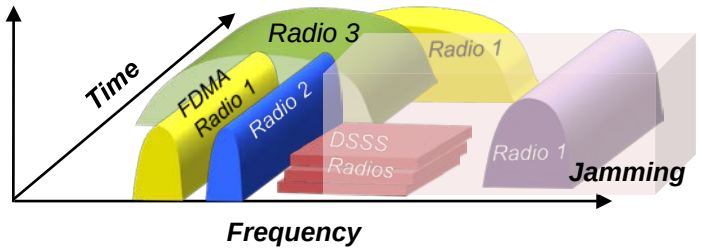
2.1 mW versus 56 mW in digital = 27x savings per channel

17 mW versus 448 mW in digital = 27x savings 8 channel chip

Motivation: Conventional digital receiver processing versus ICA chip

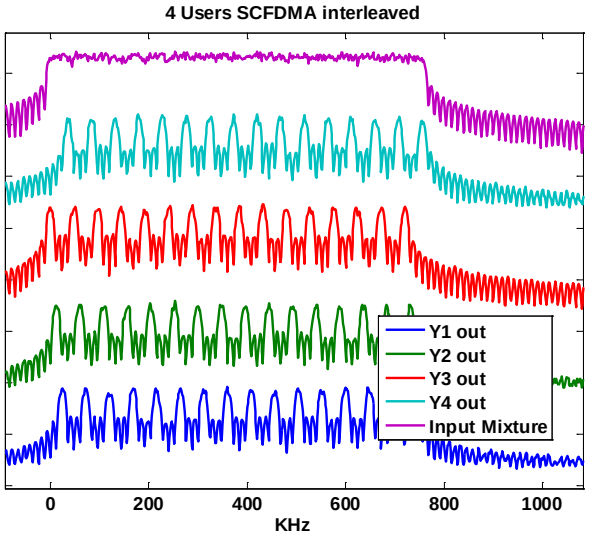
Problem: Unknown signal modulations hard to sort and segment

- Power-expensive computations required to sort and error prone



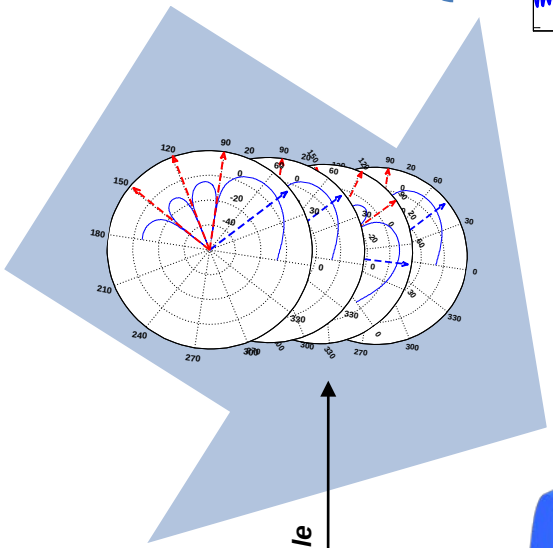
4G LTE-like uplink spectrum

ICA-based signal sorting

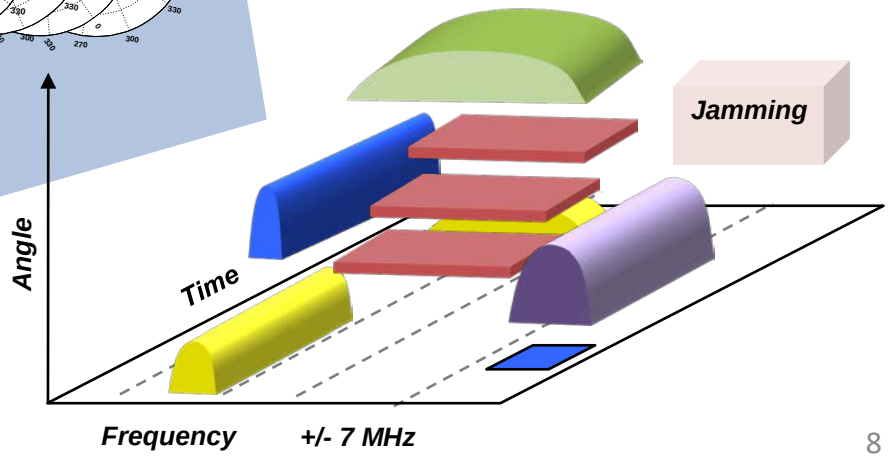


ICA chip

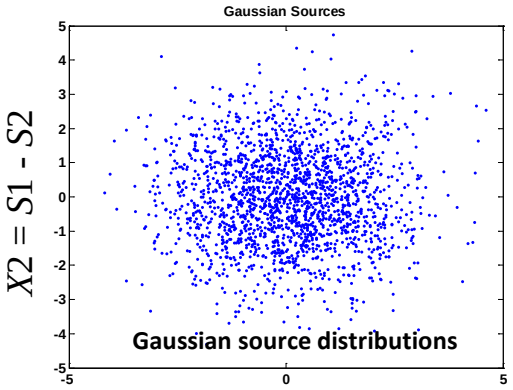
- Signals separate in angle with ICA adaptive nulling
  - **Metric for sinusoidal sources is suppression ratio (dB)**
- ICA-chip simplifies segmentation, low-power, carrier invariant
- Works in EW and cognitive radio environment



Separated and segmented signals

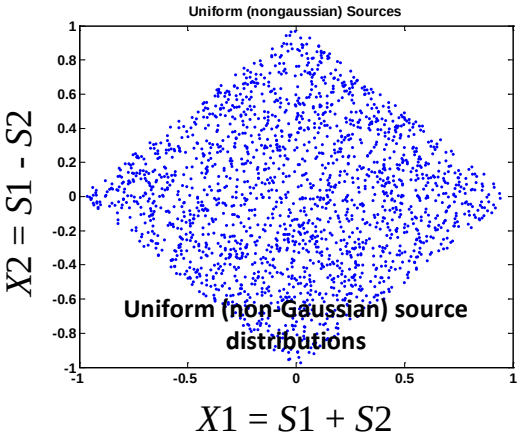


Principles of ICA for blind-source separation of signals



$$X1 = S1 + S2$$

$$X2 = S1 - S2$$



Definition of Statistical Independence

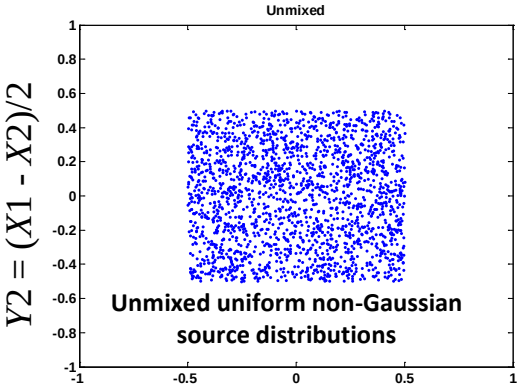
$$P(Y_1, Y_2) = \mathrm{P}(Y_1)\,\mathrm{P}(Y_2)$$

$$P(Y_1 | Y_2) = \mathrm{P}(Y_1)$$

$$\mathbf{S}(t) = \mathbf{W}\mathbf{X}(t) = \mathbf{A}^{-1}\mathbf{X}(t)$$

$$\mathbf{Y}(t) = \begin{bmatrix} 0.5 & 0.5 \\ 0.5 & -0.5 \end{bmatrix} \mathbf{X}(t)$$

- Compare instantaneous voltages received in two channels (i.e. two antennas)
- *Linear* mixtures of *independent* sources can be recognized by conditional dependence properties (except for Gaussian distributed case)
- Mixtures of non-Gaussian sources can be distinguished from shape of joint distribution
  - Requires going beyond 1st order correlations



ICA blind learning algorithm

- "Natural Gradient Infomax"
- Algorithm increments unmixing matrix **W**, based on feedback of output signals
- Uses nonlinear cross-correlation of "unmixed" signals
- Similar to whitening filter, but with higher order statistics
- Particular update rule derivable from max likelihood and independence assumption

- **W** adaptation reaches fixed point when outputs are non-linearly decorrelated
- **W** row vectors have rotated to align axis of distribution
- Output signals are now independent and normalized
- Each weight vector implements projection (to remove other independent sources) and boosting of residual signal to unit normalization

"Unmixed" signals $\vec{y}(t) = \mathbf{W}\vec{x}(t)$

$$\mathbf{W} \rightarrow \mathbf{W} + \mu\left(1 - f\left(\vec{y}(t)\right)\vec{y}(t)^T\right)\mathbf{W}$$

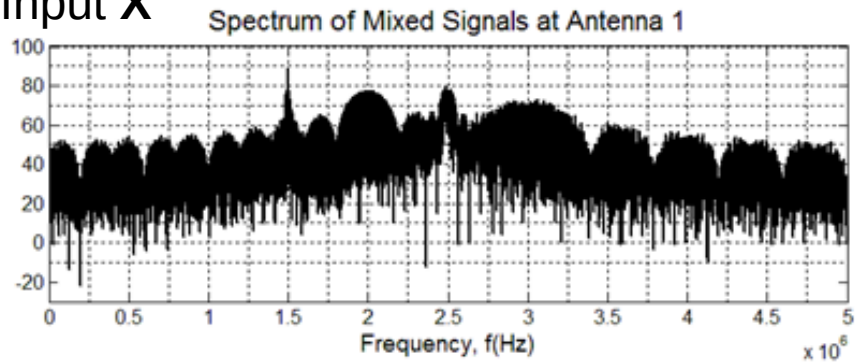
Learning rate parameter

Sub-Gaussian (communications) $f(y) = y^3$

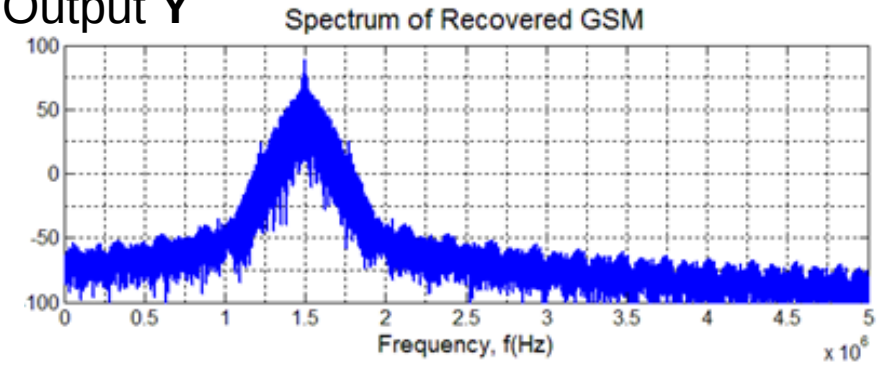
Example of MATLAB-simulated ICA operation with *N*=4 antennas

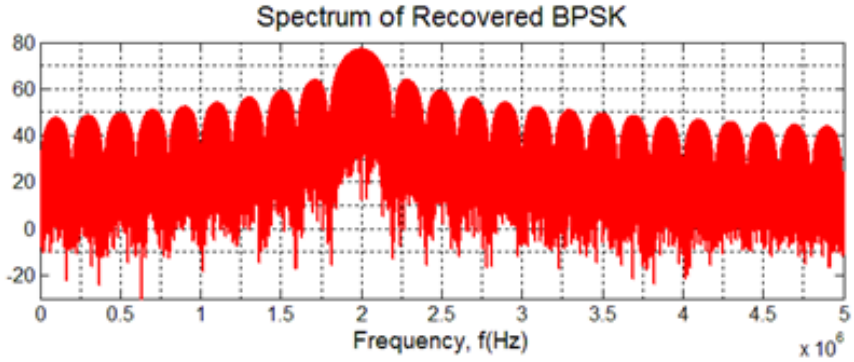
- 4 down-converted waveforms unmixed by ICA
  - GSM at f_1=1.5 MHz (270.8 kb/s)
  - BPSK at f_2=2 MHz (200 kb/s)
  - 16-QAM at f_3=2.5 MHz (270.8 kb/s)
  - SC-CDMA at f_4=3 MHz (4 users, 200 kb/s)
- Works as well for f_1=f_2=f_3=f_4

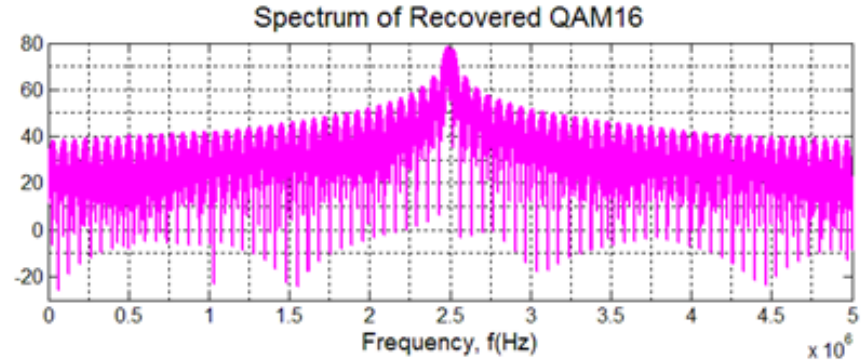
Input **X**

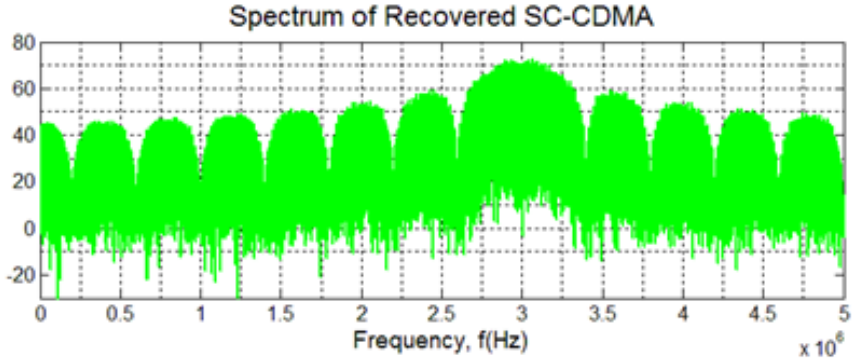


Output **Y**



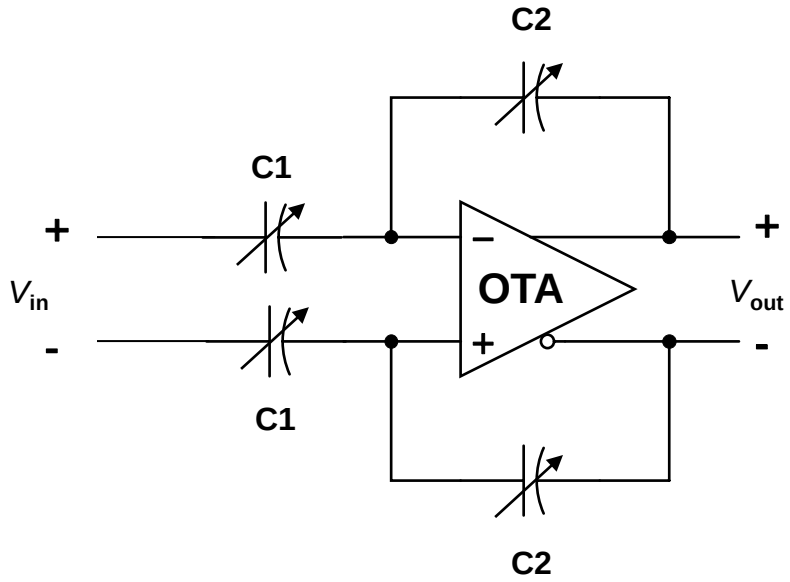






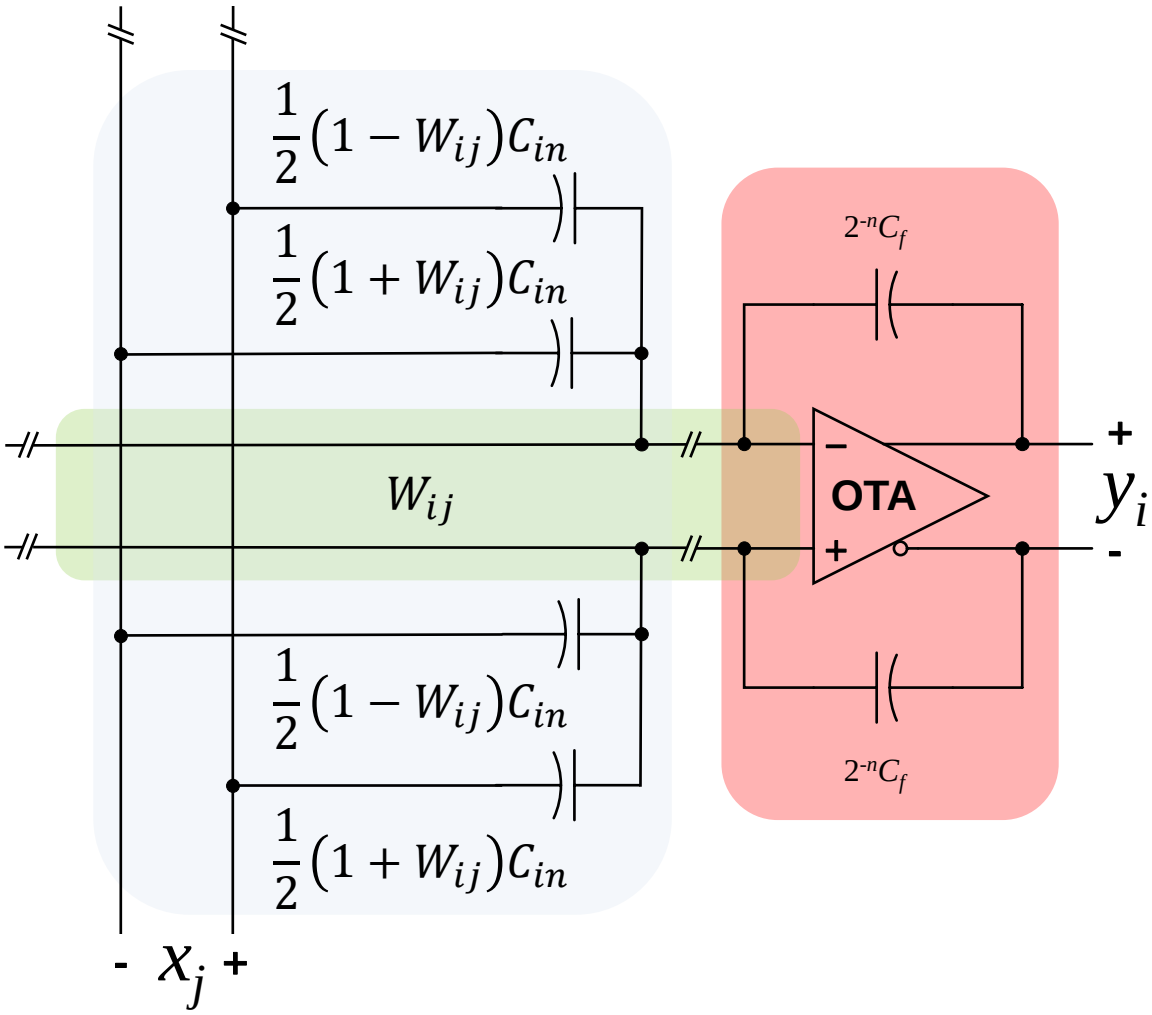
Motivation of multiplier circuit

- Core multiply-accumulate function $y_i = \sum_j W_{ij} x_j$ can be reduced to well understood summation (Σ) and multiplication ($W_{ij}x_j$) opamp-based realizations
- Conceptual circuit on right shows functional realization of multiplication as V_{out}/V_{in} = C1/C2.
  - Operational transimpedance amplifier (OTA) input is virtual node for input current summation from multiple input paths
  - Use of capacitive elements allows implementation to achieve matching limited by metal lithography and oxide-thickness variation across the chip
  - Well-understood switched-capacitor realization (dating back to CMOS audio-circuits in the 1980s) enables realization with desirable properties of mismatch and noise compensation



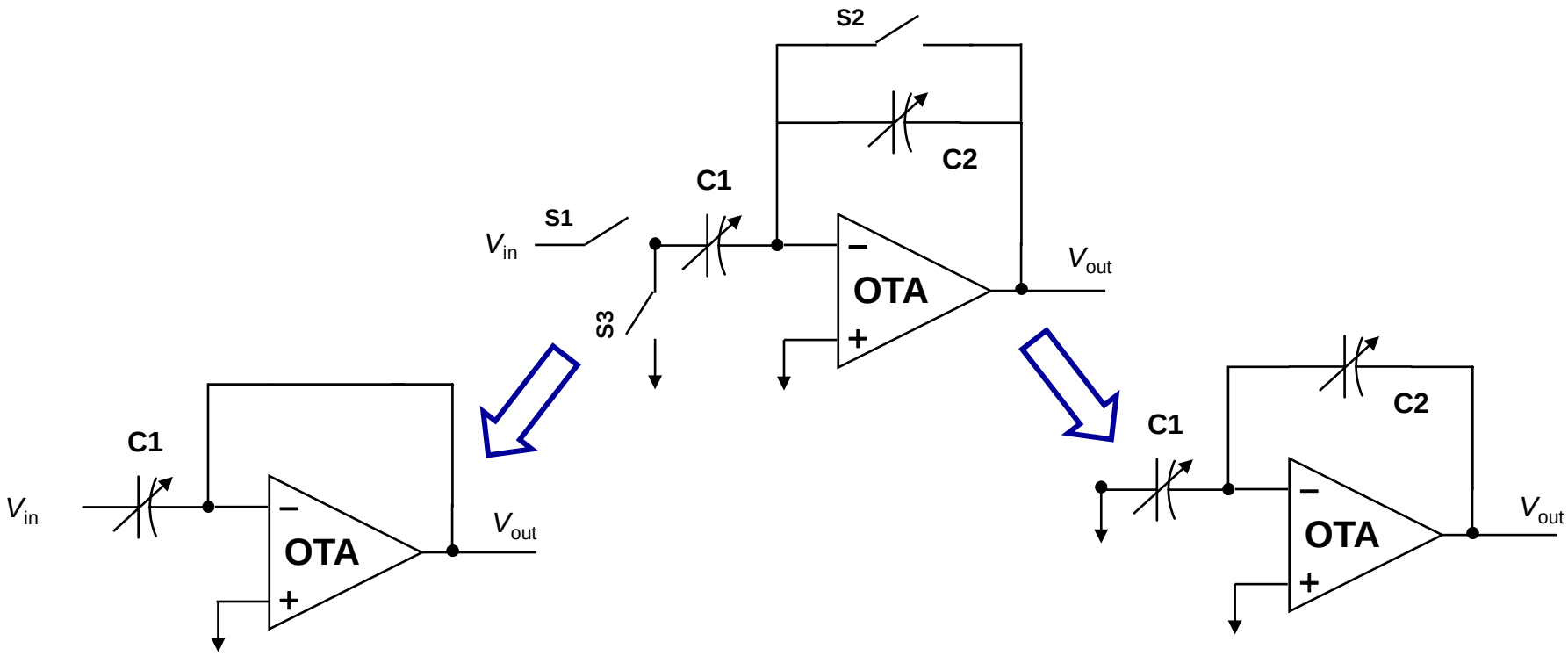
ICA multiply-accumulate (MAC) core

- Conceptual top-level functional block diagram of single-channel, differential multiply-accumulate function with 8 inputs (x_j, j=1..8) and output y_i
- Input weights are differential, guaranteed monotonic 13-bit digitally programmable weights W_{ij}, matched to within +/- 3% across process variation and temperature (PVT)
- Signal path gain can be selected to be 1x or 2x by 1-bit programmable $2^{-n}C_f$
  - 1x default to preserve 10-bit linearity of signal path
  - 2x may be selected to boost ICA core signal amplitude for small angle-separation of inputs.



$$y_i = \frac{\sum_j W_{ij} C_{in} x_j}{2^{-n} C_f} = \frac{C_{in}}{C_f} 2^n \sum_j W_{ij} x_j$$

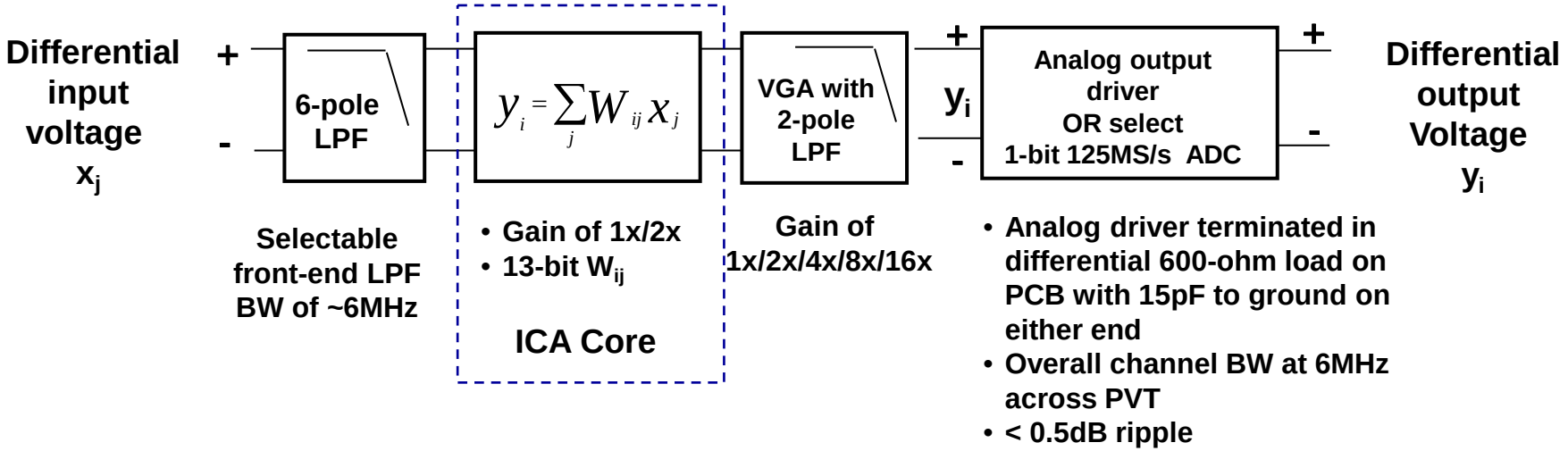
Motivation – operation of switched-capacitor multiplier circuit



Effective circuit during the "**'sampling phase**".
Switches S1, S2 are closed and S3 is open.
During this phase, the input signal is sampled onto capacitor C1, which develops V_{in}, within the error of the OTA that maintains a virtual small-signal ground at the negative input terminal of the OTA.

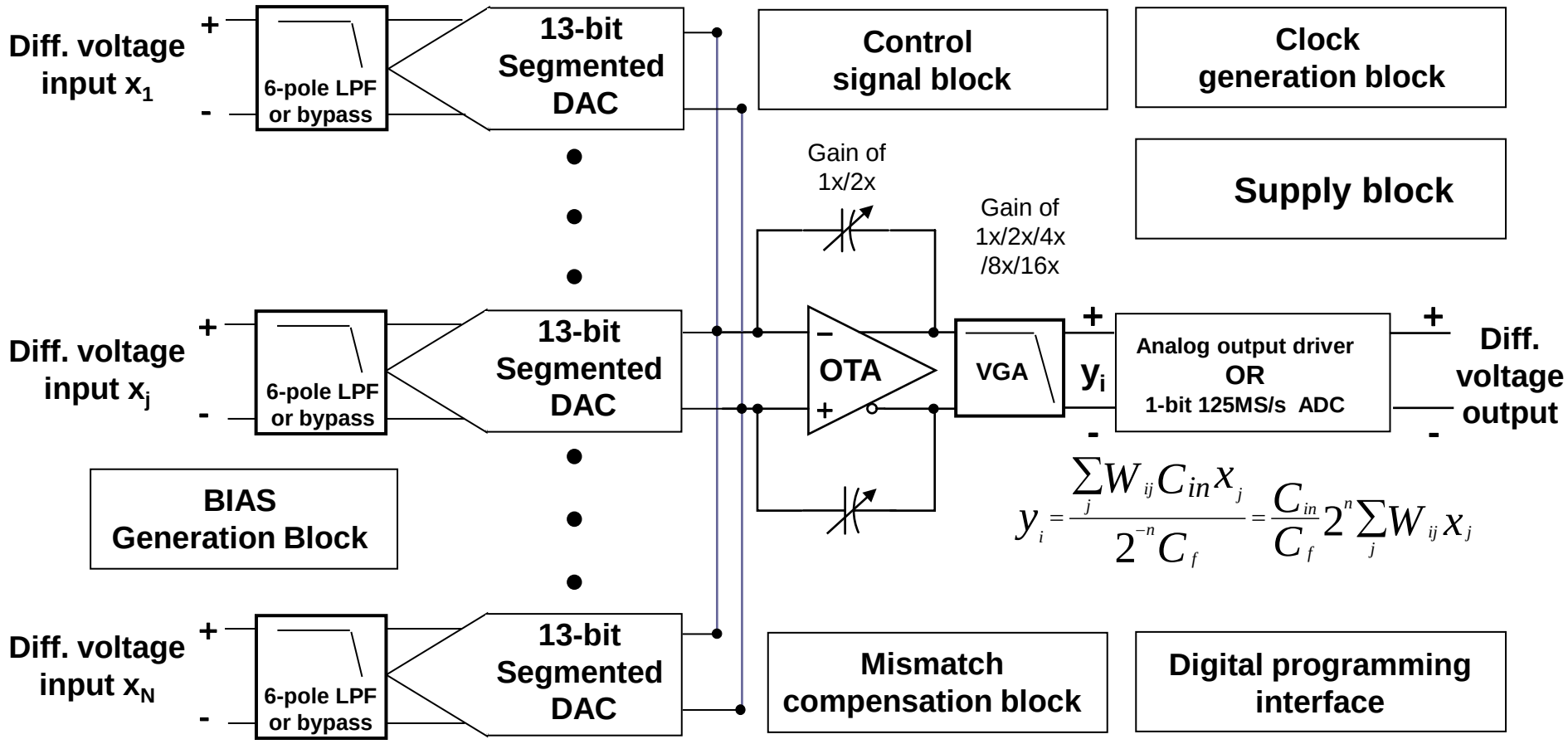
Effective circuit during the "**amplification phase**".
Switches S1, S2 are open and S3 is closed.
During this phase, the voltage across capacitor C1 is approximately 0V (within the error of the OTA), which causes the charge accumulated in C1 to flow into capacitor C2, causing V_{out} = (C1/C2) V_{in}.

Design approach and specification



- Production-quality design across process variation and temperature (PVT)
- Test chip specific LPF and output driver, not relevant on platform IC
- Short design cycle time => maximal schematic and layout reuse
- Available process through MOSIS does not have High Performance Analog Transistors
- Guaranteed linearity (IM3 two-tone tests) better than 63 dB (10-bits) across PVT at 1Vpp
- Input-referred noise no worse than 300μVrms
- Guaranteed channel matching within +/- 3% across PVT
  - Designed to be within +/- 1% without calibration
  - Channel bandwidth to be ~6MHz nominal
  - < 0.5 dB ripple
- 13-bit weights W_{ij} consisting of sign bit and 12 magnitude bits, no calibration
  - Guaranteed monotonic weights
  - Segmented C-segmented R DACs, time constant >> 6MHz => small R => LPF requires large current to establish large output voltage and maintain 63dB linearity

ICA chip top-level simulation schematic diagram



The linear mixing matrix **A** gives complex RF input signals **X** = **AS**

We seek the unknown original complex signals **S** = $\mathbf{A}^{-1}\mathbf{X}$

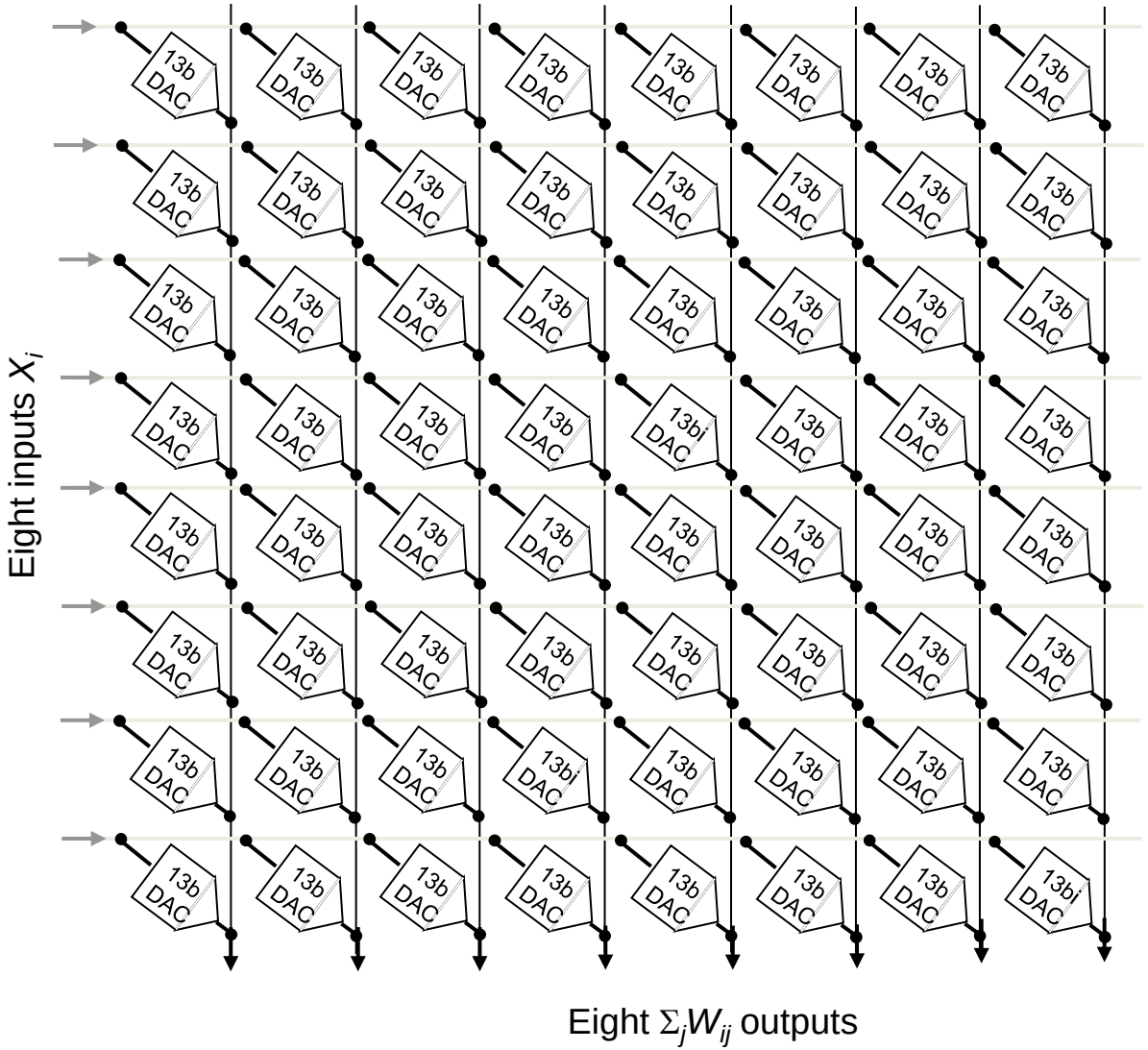
ICA blind-source separates the input signal **X** by unmixing the linear combination to give **Y** = **WX**

where **W** approximates $\mathbf{A}^{-1}$ and **Y** approximates **S**

The ICA chip does this unmixing before ADC and DSP

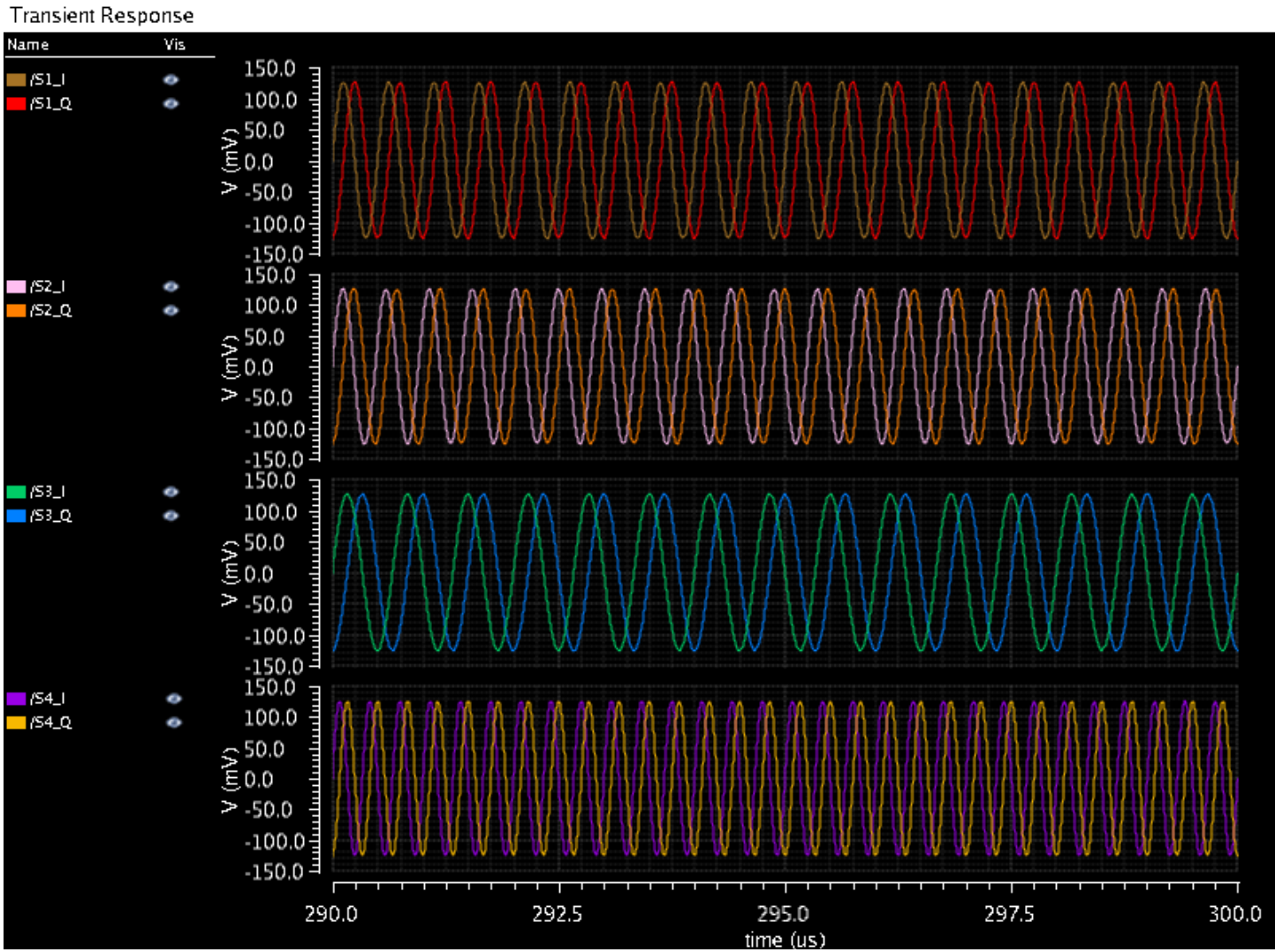
ICA chip 8 x 8 W_{ij} weight matrix in ICA

- Conceptual top-level functional block diagram of 8 x 8 W_{ij} weight matrix in ICA chip core.
- Implementation requires differential, guaranteed monotonic 13-bit (sign bit + 12 magnitude bits) weights W_{ij}, for a total of sixty-four (64) digitally programmable weights, matched to within +/- 3% across PVT.
- The differential digitally programmable matrix weight array is implemented (designed and drawn) on-chip as a segmented 6-bit *R* (lsb), 6-bit *C* (msb) array.



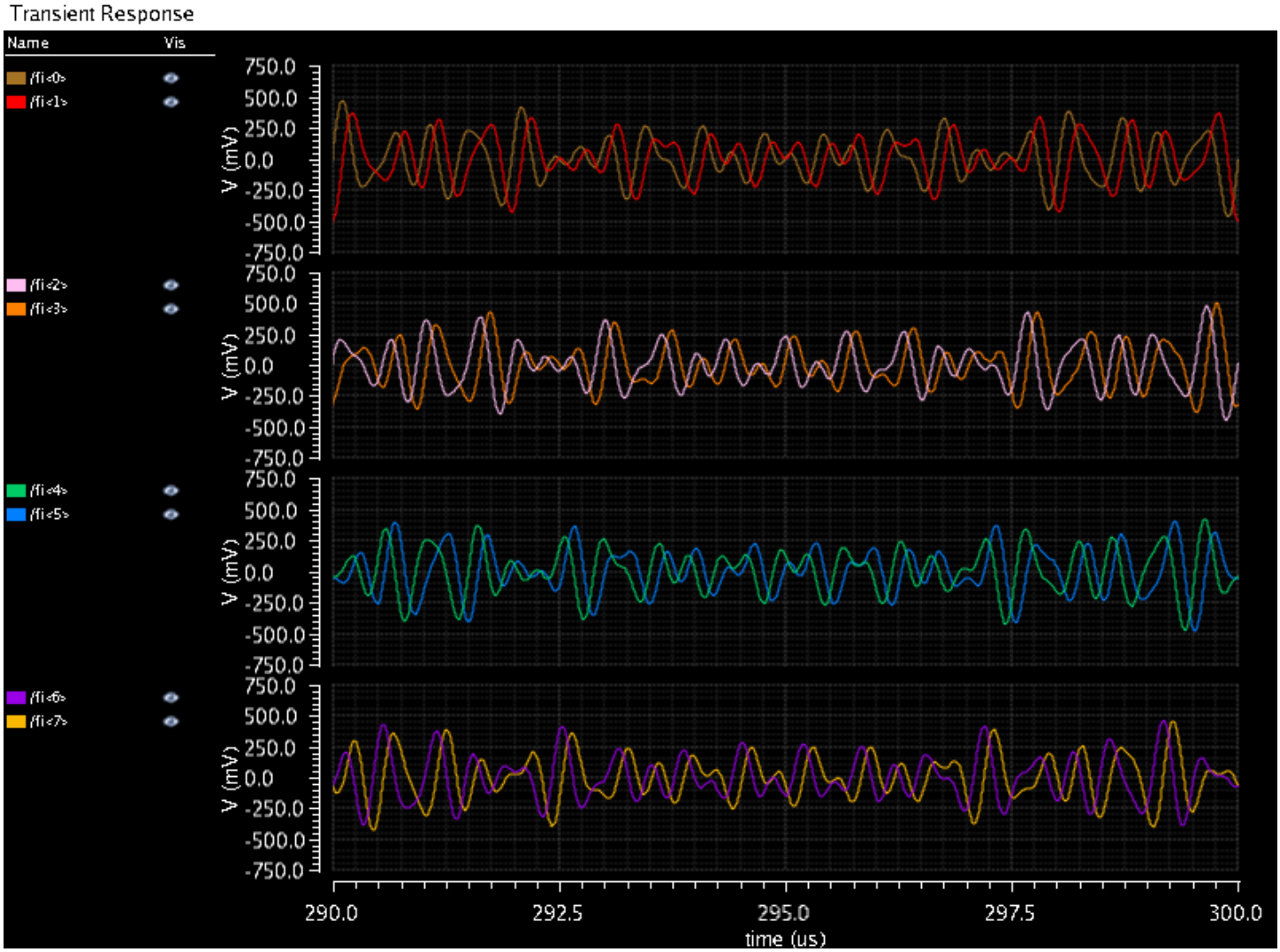
Example 4-antenna separation details of HSPICE simulation

- S-inputs, 200mVpp
- S1_I,Q=2.0MHz
- S2_I,Q=2.1MHz
- S3_I,Q=1.5MHz
- S4_I,Q=3.0MHz
- ϕ_1= +0°, ϕ_2= +1.3°, ϕ_3= -65°, ϕ_4= +80°
- Weight matrix from Test16 MATLAB file



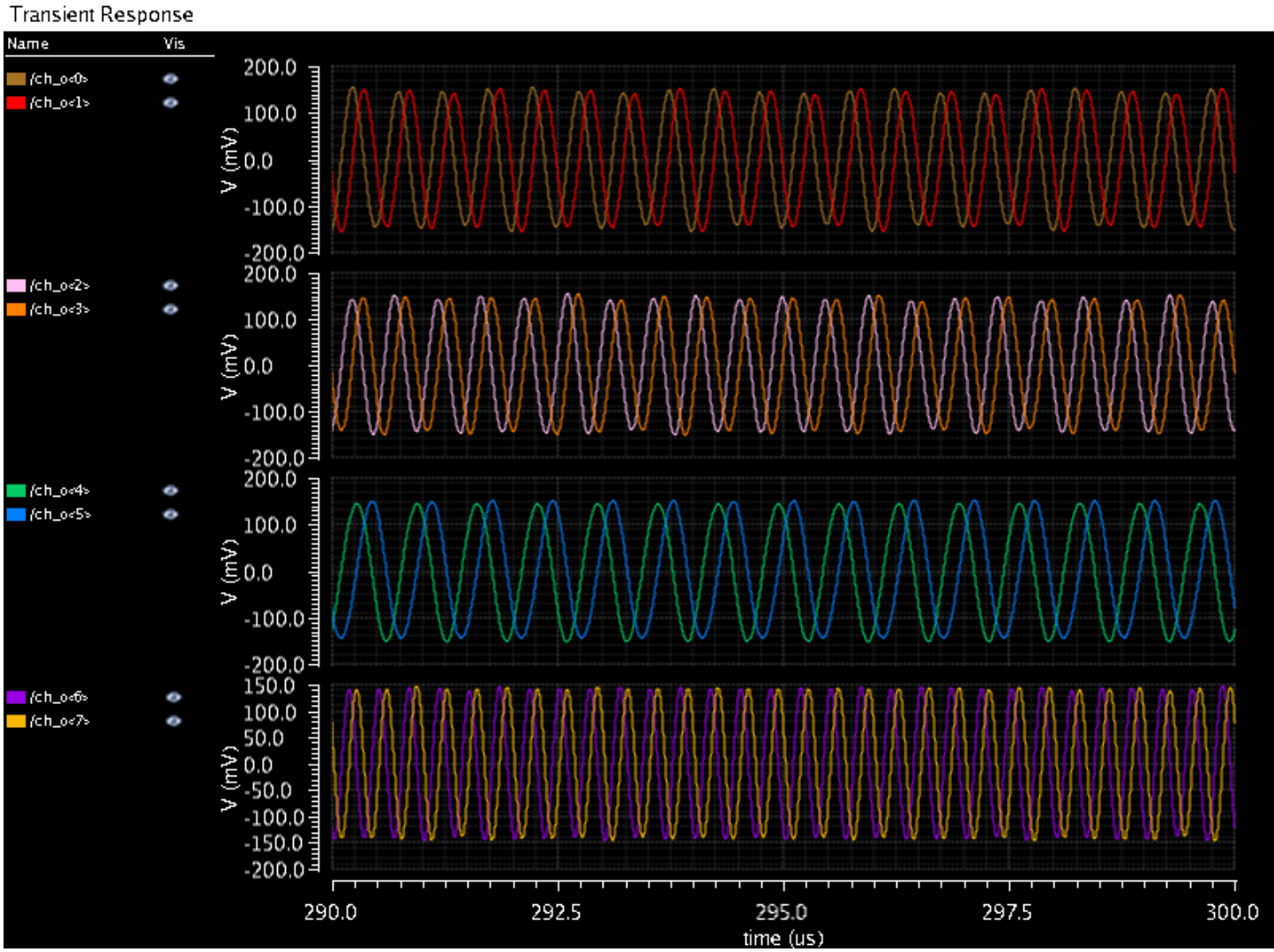
Mixed X-inputs, <= 1Vp-p

- S1_I,Q=2.0MHz
- S2_I,Q=2.1MHz
- S3_I,Q=1.5MHz
- S4_I,Q=3.0MHz
- ϕ_1= +0°, ϕ_2= +1.3°, ϕ_3= -65°, ϕ_4= +80°
- Weight matrix from Test16 MATLAB file

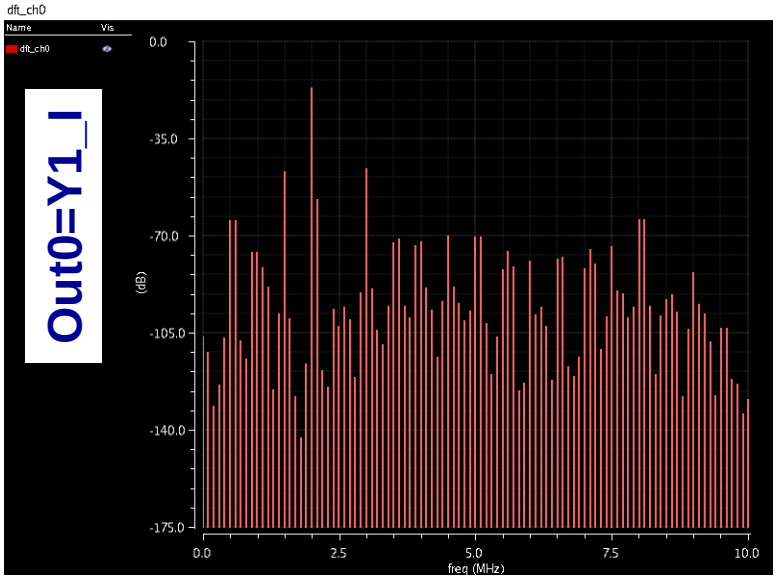


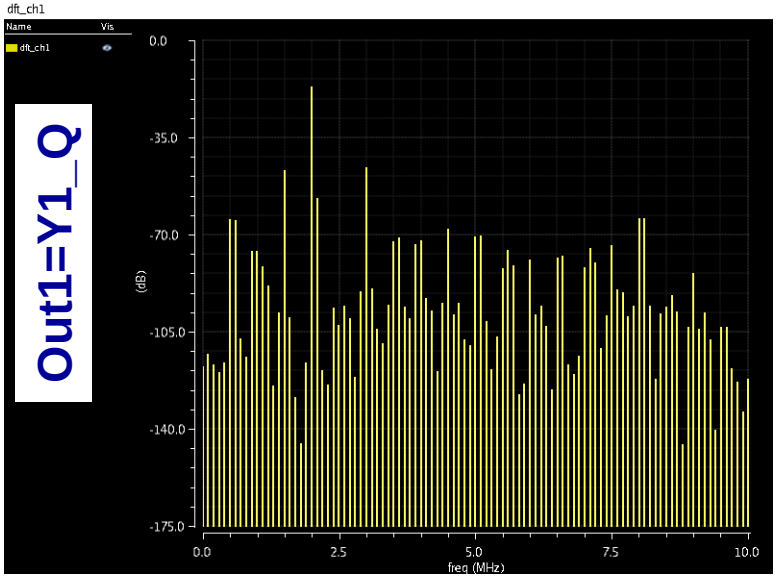
Unmixed Y-Outputs, ~300mVp-p

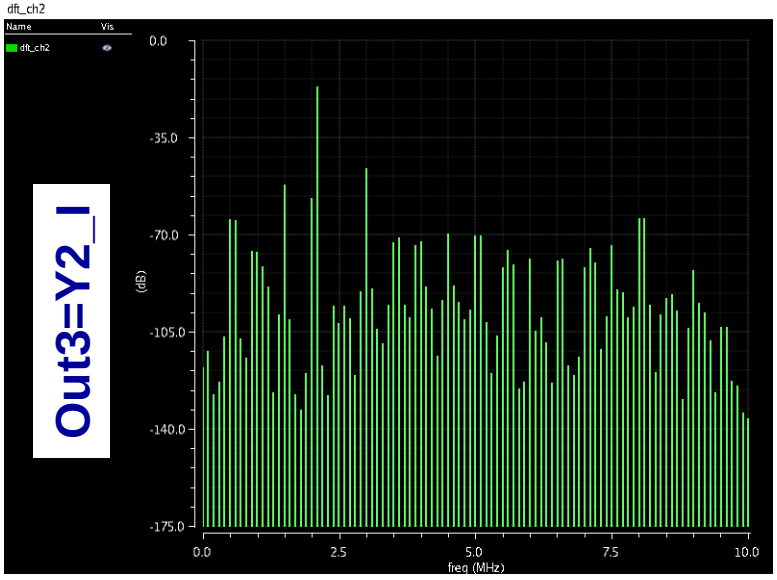
- S1_I,Q=2.0MHz
- S2_I,Q=2.1MHz
- S3_I,Q=1.5MHz
- S4_I,Q=3.0MHz
- ϕ_1= +0°, ϕ_2= +1.3°, ϕ_3= -65°, ϕ_4= +80°
- Weight matrix from Test16 MATLAB file
- Gain for all paths, 30dB

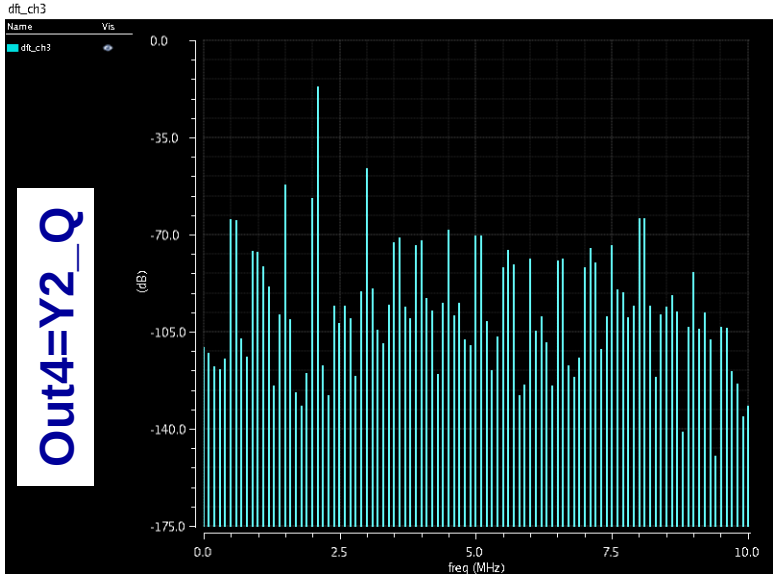


DFT of first set of four Y outputs

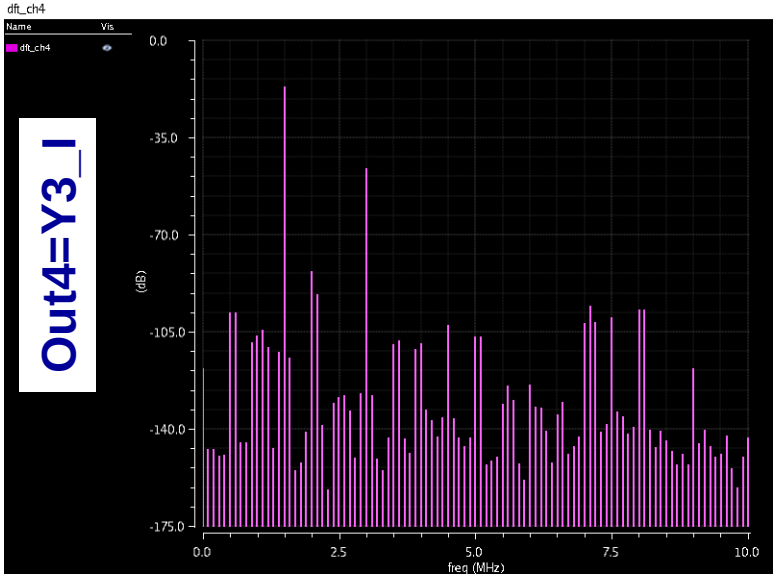


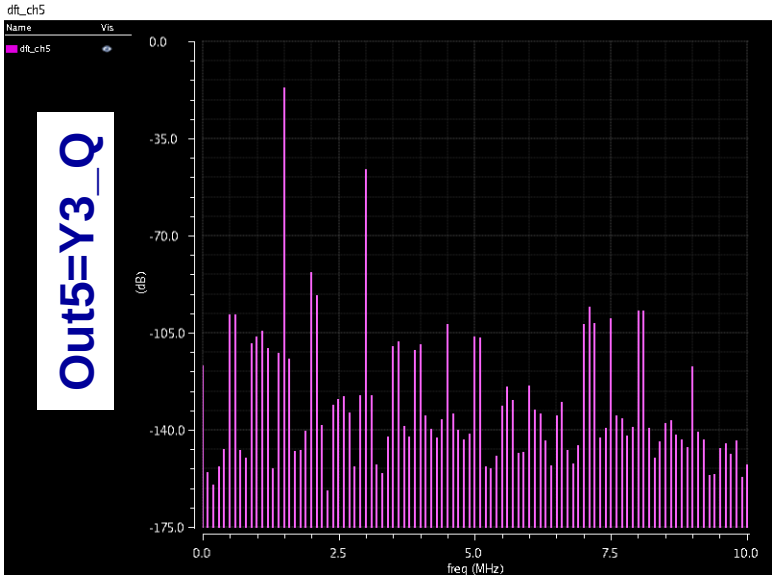


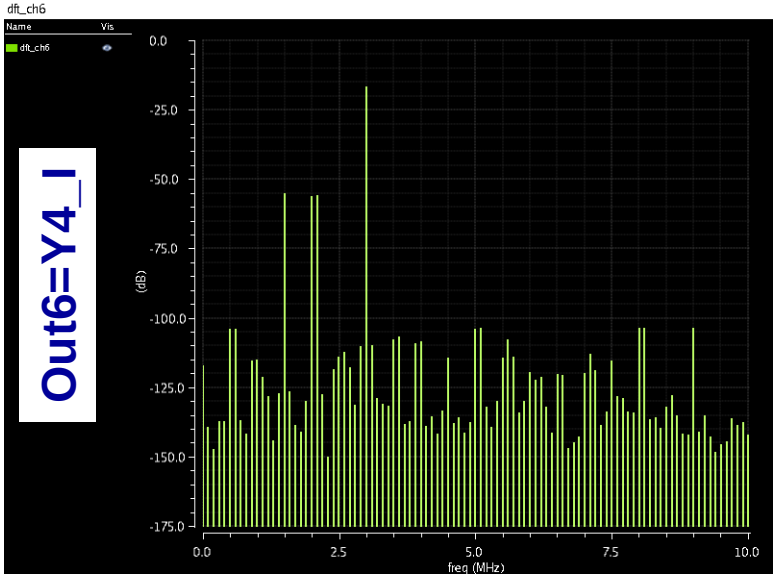


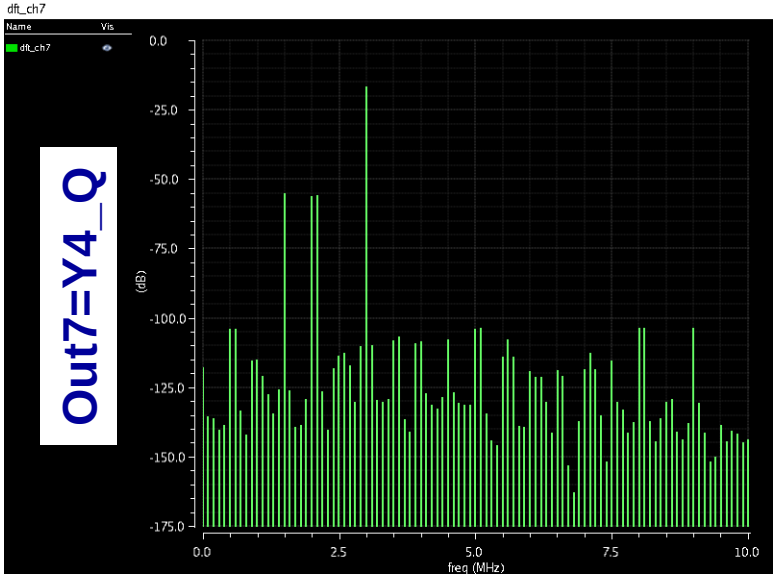


DFT of second set of four Y outputs









4-antenna HSPICE simulation unmixing results

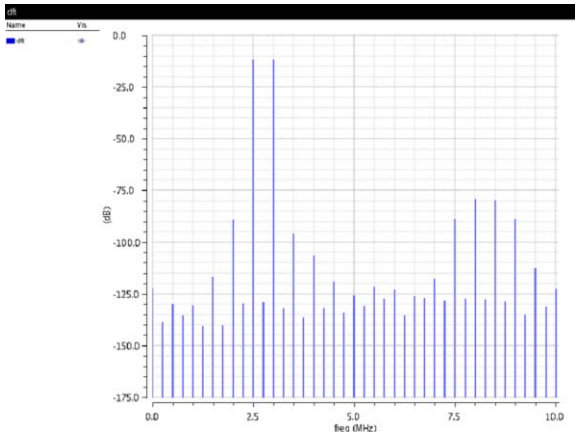
- Optimized weights from MATLAB analytic model ϕ_1= +0°, ϕ_2= +1.3°, ϕ_3= -65°, ϕ_4= +80°
- 300us transient simulation.
- DFT from 290us to 300us.
- Simulation time is ~60us/hour (wall-time) -- CPU-bound.
- Upper table is Typical transistor, resistor, capacitor corner (TT), 27C, 1.2V
  - Worst-case channel suppression is –29.14dB
- Lower table is Slow P, Slow N transistor corner (SSF), Max resistor and Max capacitor corner, 125C, 1.13V (4.9 parts per billion failure rate)
  - Worst-case channel suppression is –27.67dB

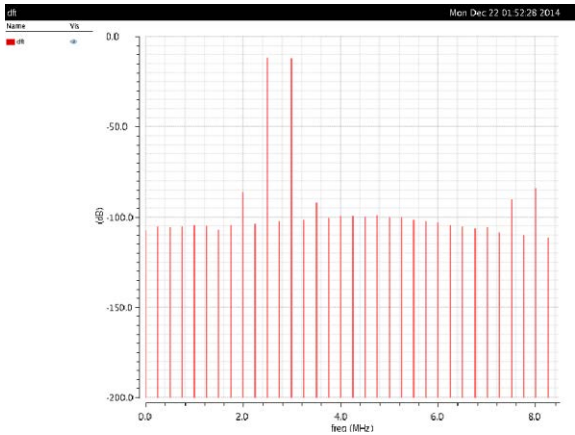
Channels	Desired Signal Frequency (MHz)	Desired Signal Strength (dB) in DFT	Largest undesired Signal Frequency (MHz)	Highest Undesired Signal Strength (dB)	Worst-case Suppression (dB)
out0	2	-16.73	3	-45.87	-29.14
out1	2	-16.73	3	-45.87	-29.14
out2	2.1	-16.80	2	-46.17	-29.37
out3	2.1	-16.80	2	-46.17	-29.37
out4	1.5	-16.69	3	-46.18	-29.49
out5	1.5	-16.69	3	-46.18	-29.49
otu6	3	-16.91	1.5	-55.17	-38.26
out7	3	-16.91	1.5	-55.17	-38.26

Channels	Desired Signal Frequency (MHz)	Desired Signal Strength (dB) in DFT	Largest undesired Signal Frequency (MHz)	Highest Undesired Signal Strength (dB)	Worst-case Suppression (dB)
out0	2	-17.07	1.5	-46.63	-29.55
out1	2	-17.07	1.5	-46.63	-29.55
out2	2.1	-17.15	3	-47.30	-30.15
out3	2.1	-17.15	3	-47.30	-30.15
out4	1.5	-17.00	3	-44.67	-27.67
out5	1.5	-17.00	3	-44.67	-27.67
otu6	3	-17.29	2.1	-54.19	-36.90
out7	3	-17.29	2.1	-54.19	-36.90

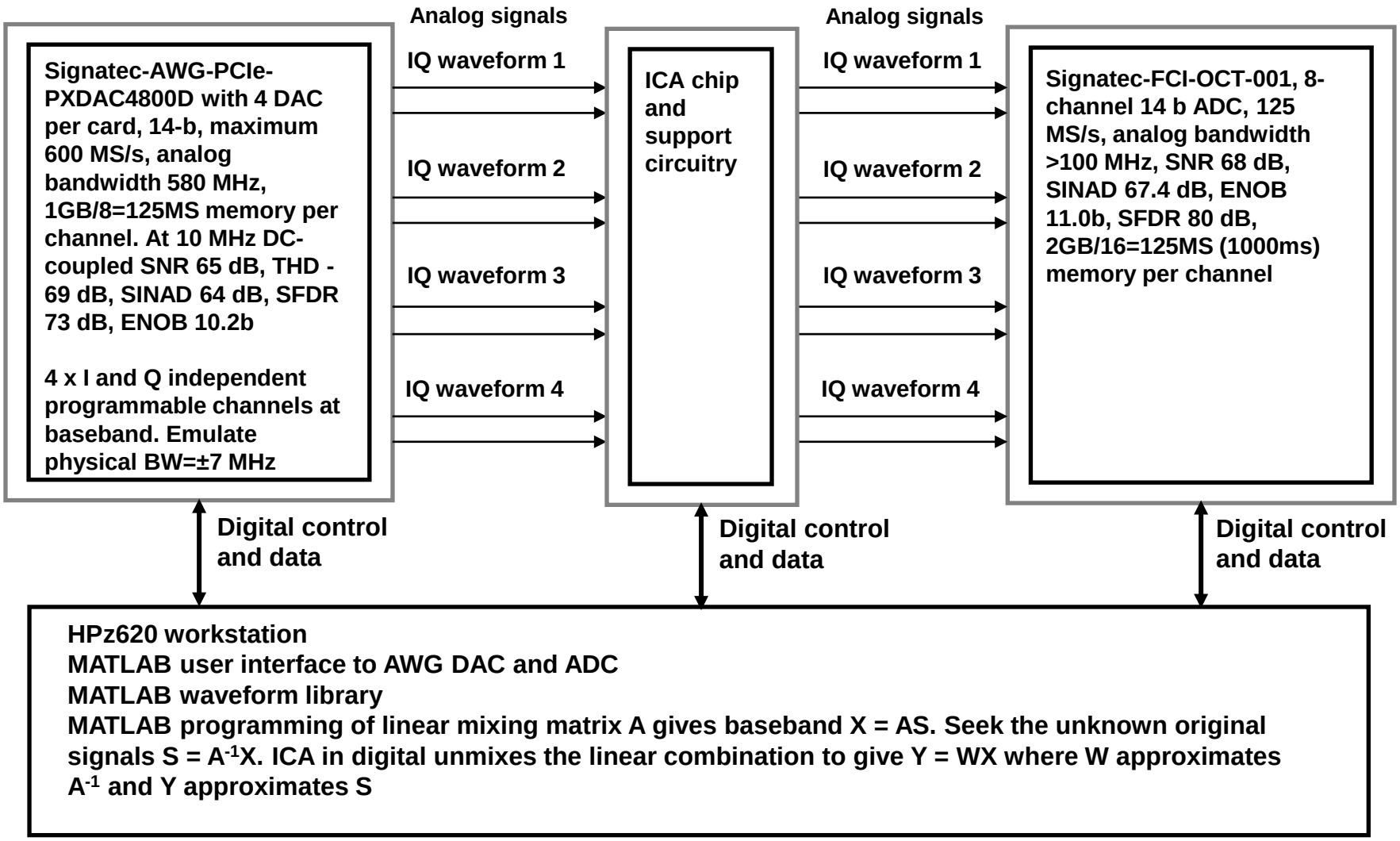
Typical HSPICE two-tone linearity test in ICA chip signal-path simulation

- Includes constant-g_m bias circuit, input 6-pole filter, and analog output driver.
- The output driver drives a differential load of 600-ohms with 15pF of capacitive load from each of the plus and minus paths to ground. The above load models the signal-load seen on the printed-circuit board (PCB).
- The input common-mode voltage (vcm) tracks changes in the supply-voltage.
- Simulation results recorded for different transistor process corners of typical (TT), worst-case slow (SSF) and worst-case fast (FFF); resistor corners of typical, max resistance and min resistance; capacitor corners of typical, maximum capacitance and minimum capacitance, junction temperature of 27°C (typical), min (-40°C) and max (125°C) and supply voltages of 1.13 V (minimum), 1.2 V (typical) and 1.26 V (maximum).
- DFT results (68.19dB linearity) of two-tone test (500 mVp-p 2.5 MHz and 3 MHz) for the typical-typical (TT) process corner (transistors, resistor and capacitor) at 27°C and V_{DD}=1.2 V.
- DFT results (71.57dB linearity) of two-tone test (500 mVp-p 2.5 MHz and 3 MHz) for the SSF transistor corner, -3 sigma resistor and capacitor corner at 125°C and VDD=1.13 V.



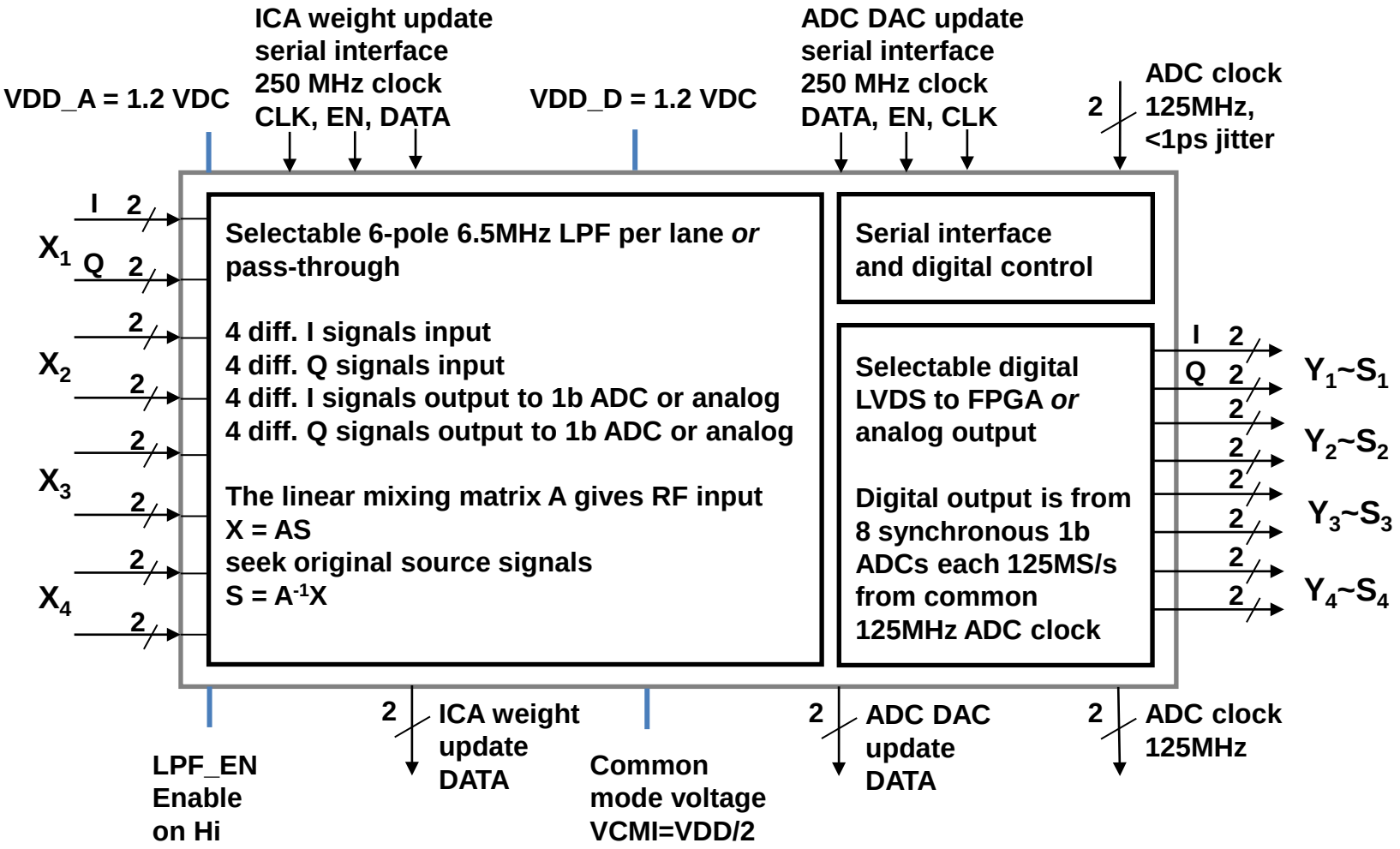


Block diagram of ***basic ICA chip test-bed***



Notes: SMA connectorized cable used in initial bench top testing.

Block diagram of ICA chip



Notes: digital data link from ADC to FPGA is 8x125Mb/s=1Gb/s. ADC DAC-threshold update rate is 500kHz max. with SPI clock at 250MHz. ICA weight-update rate is 100kHz max. with SPI clock at 250MHz.

The EN_{ADC} logic control bit set Hi in ADC serial interface selects the per-channel 125 MS/s 1-bit ADC digital output and ADC clock output. The EN_{ADC} logic control bit set Lo in ADC serial interface selects analog differential outputs and powers down the ADC clock output path. This is the default setting on power-up.

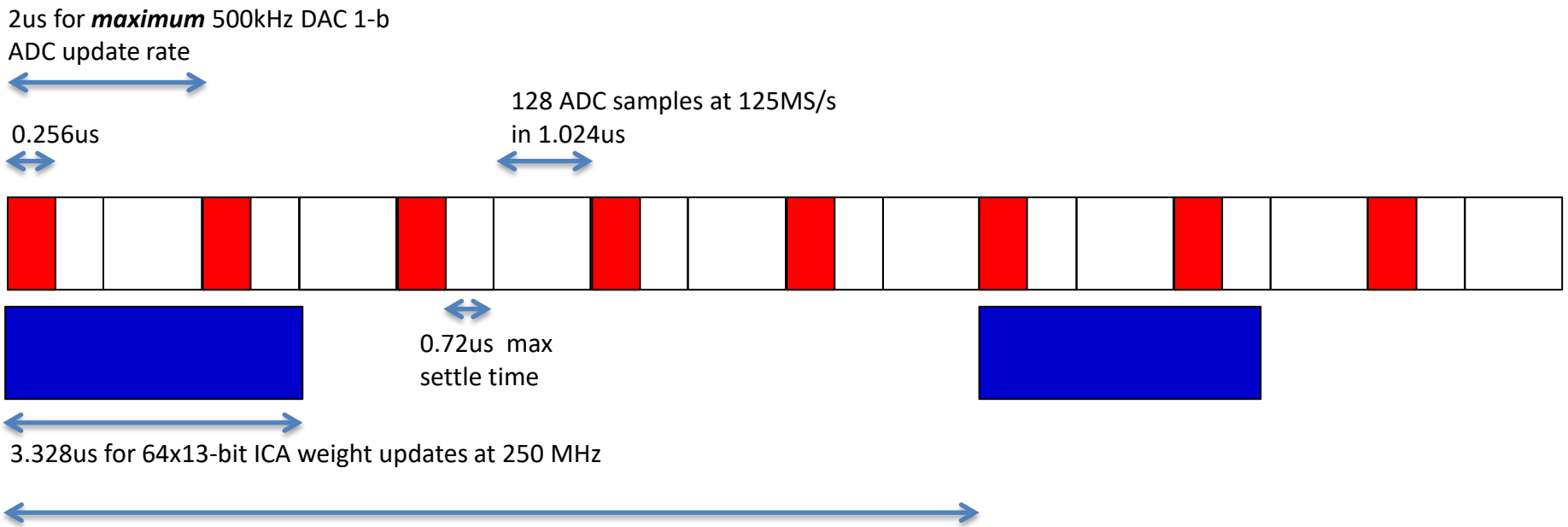
Timing: 8-b DAC 1-b ADC 500 kHz update rate and 13-b ICA weight update rate at 100 kHz (100 updates per millisecond)

8-b DAC 1-b ADC update

8bx8=64b at CLKDAC=250MHz
takes tDAC=0.256us

13-b ICA weight update

13bx32=832b at CLKWUD=250MHz
takes tWUD=3.328us



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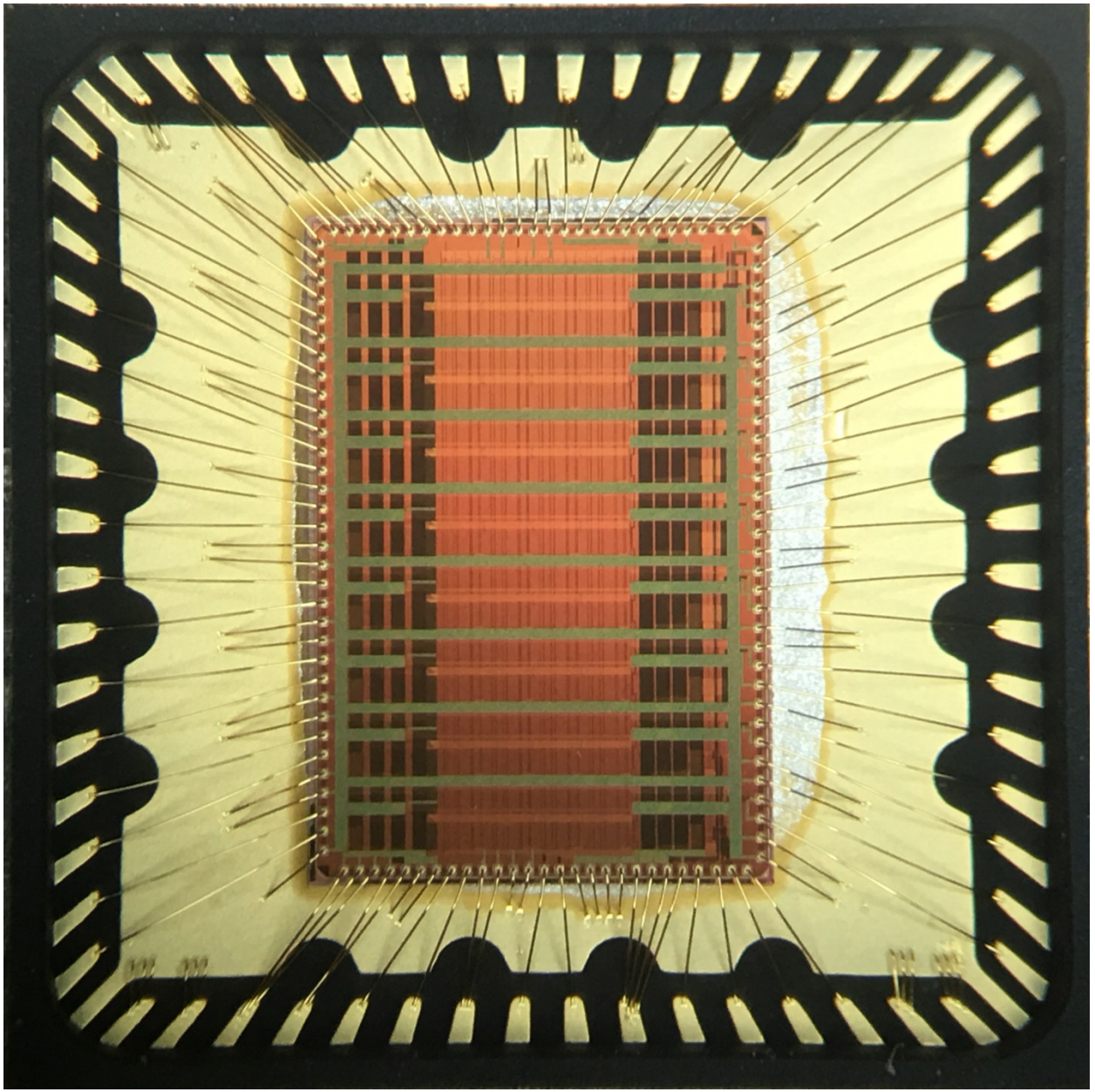
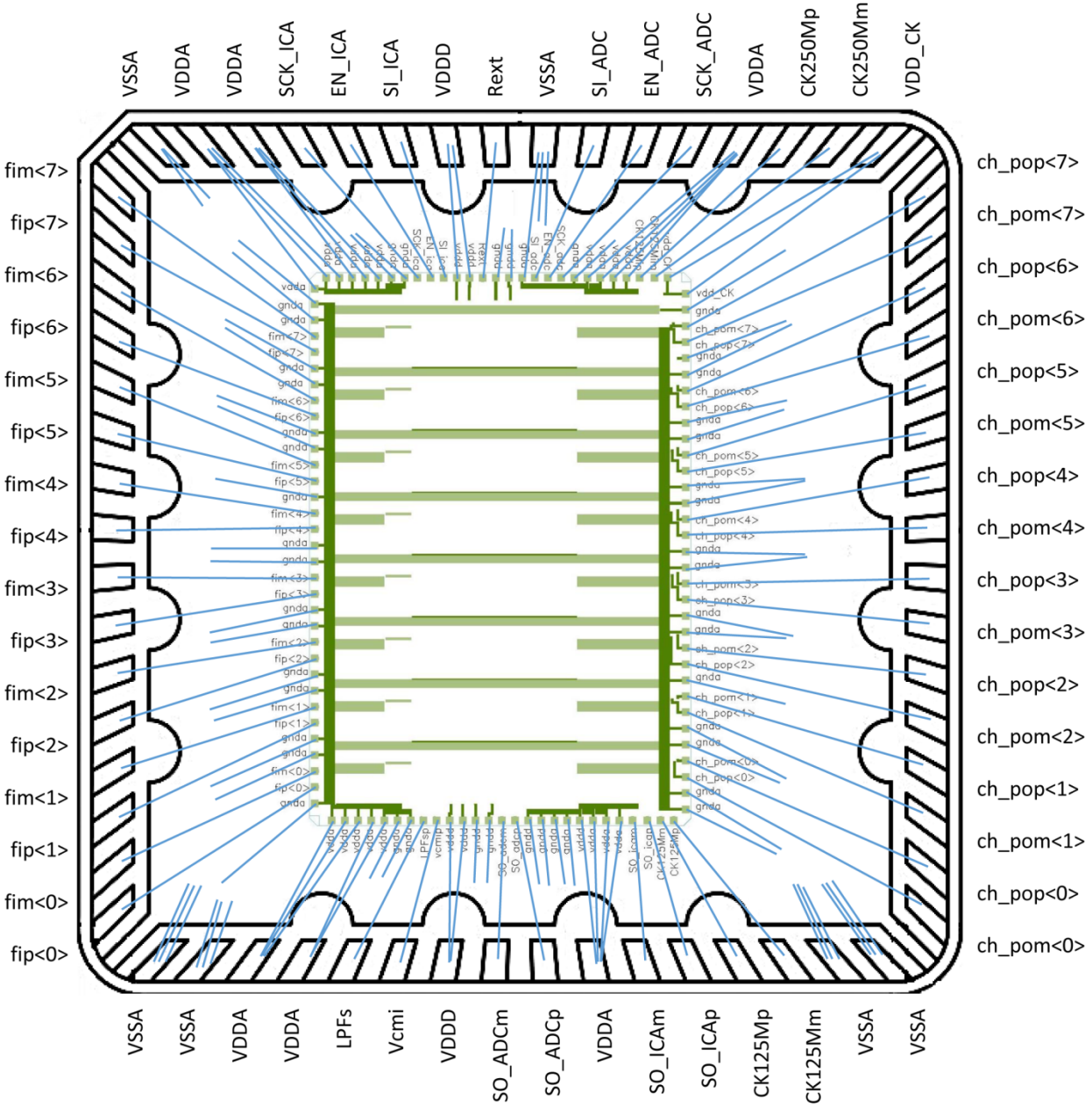
The EN_{ADC} logic control bit set Hi in ADC serial interface selects the per-channel 125 MS/s 1-bit ADC digital output and ADC clock output. The EN_{ADC} logic control bit set Lo in ADC serial interface selects analog differential outputs and powers down the ADC clock output path. This is the default setting on power-up.

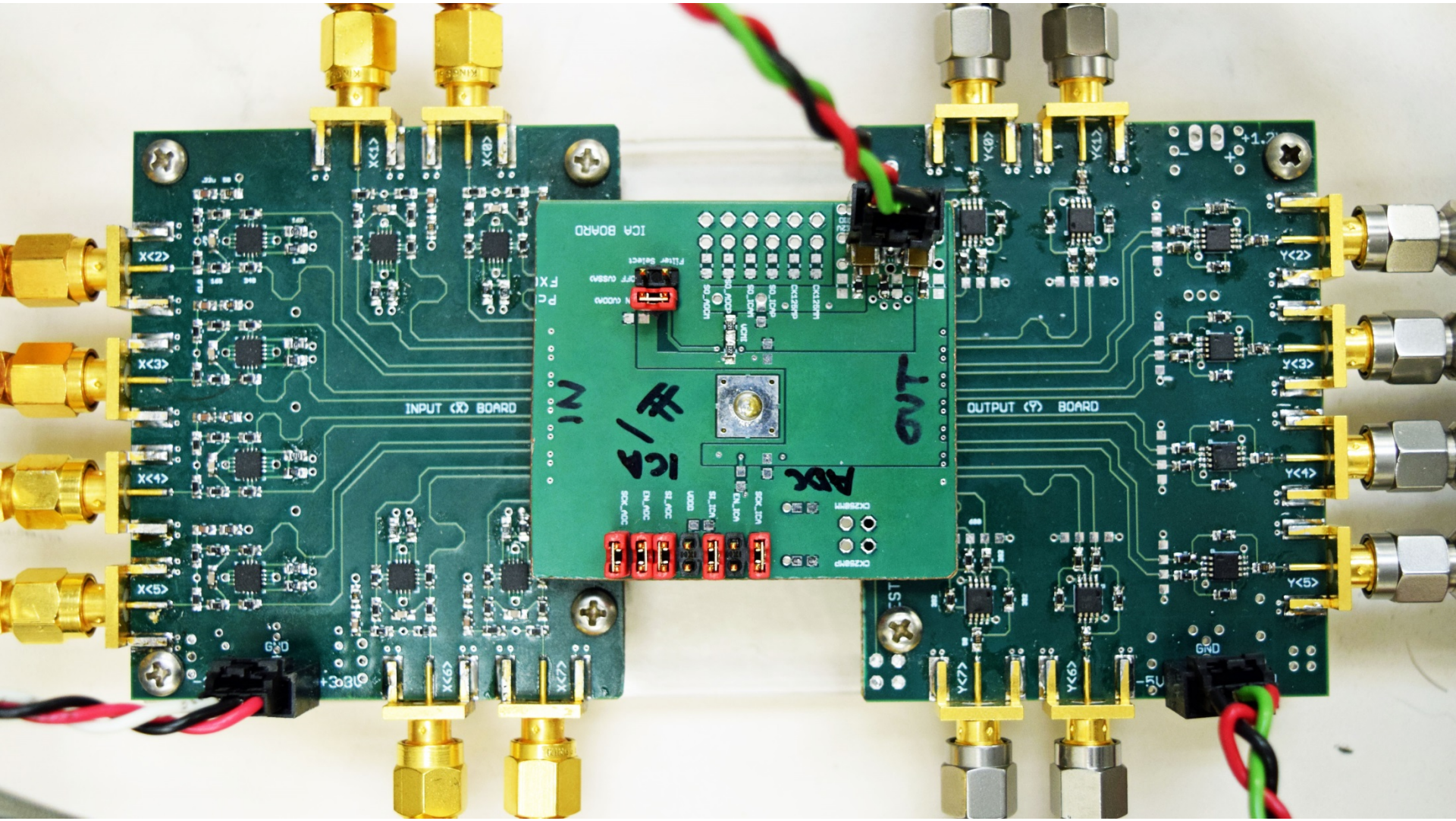
ICA chip in package



ICA chip pinout



Test setup



-1.7V, GND, +3.3V **+1.2 digital, GND, +1.2V analog** **-5V, GND, +5V**

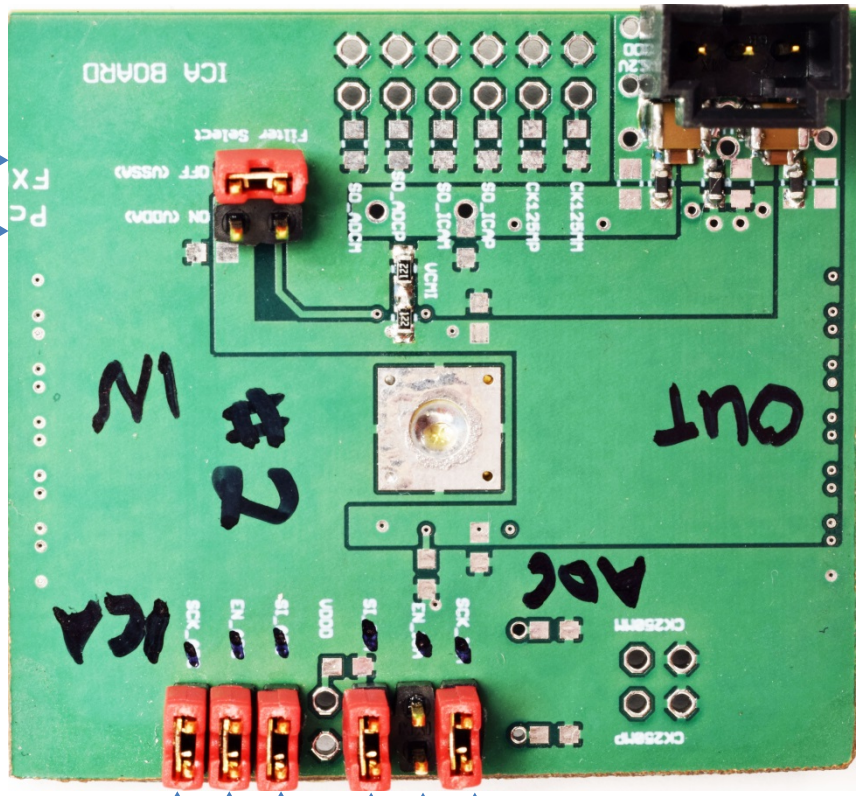
Input board ICA board Output board

ICA board

+1.2 digital, GND, +1.2V analog

Input filter off

Input filter on



In

Out

SCK_ICA

EN_ICA

SI_ICA

SCK_ADC

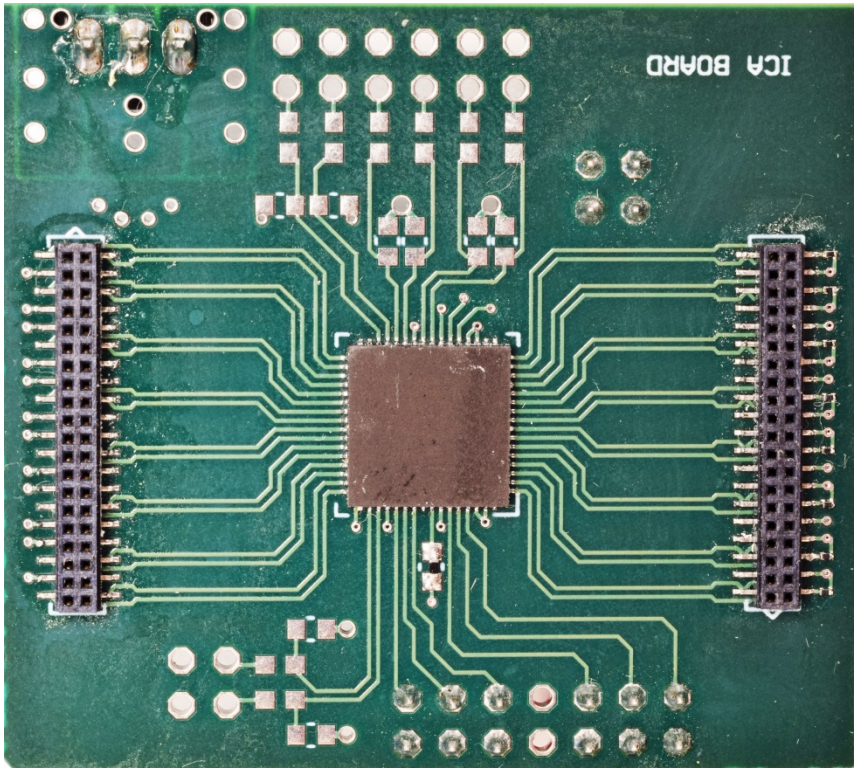
EN_ADC

SI_ADC

ICA board

+1.2 analog, GND, +1.2V digital

Out



In

SCK_ADC

EN_ADC

SI_ADC

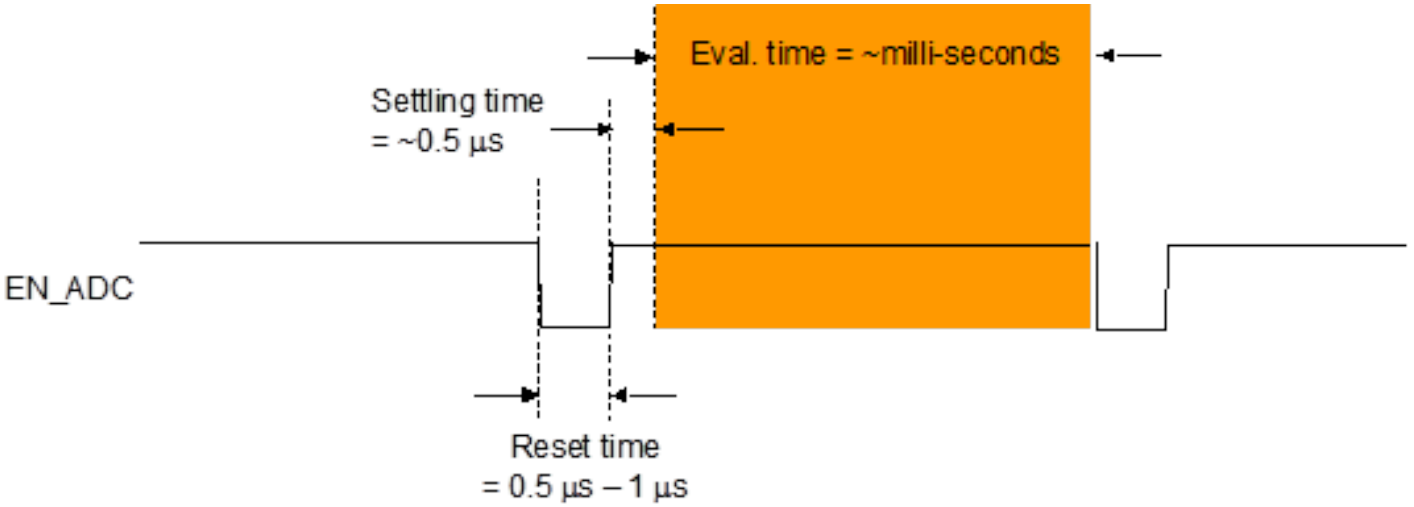
SCK_ICA

EN_ICA

SI_ICA

Initial analog tests

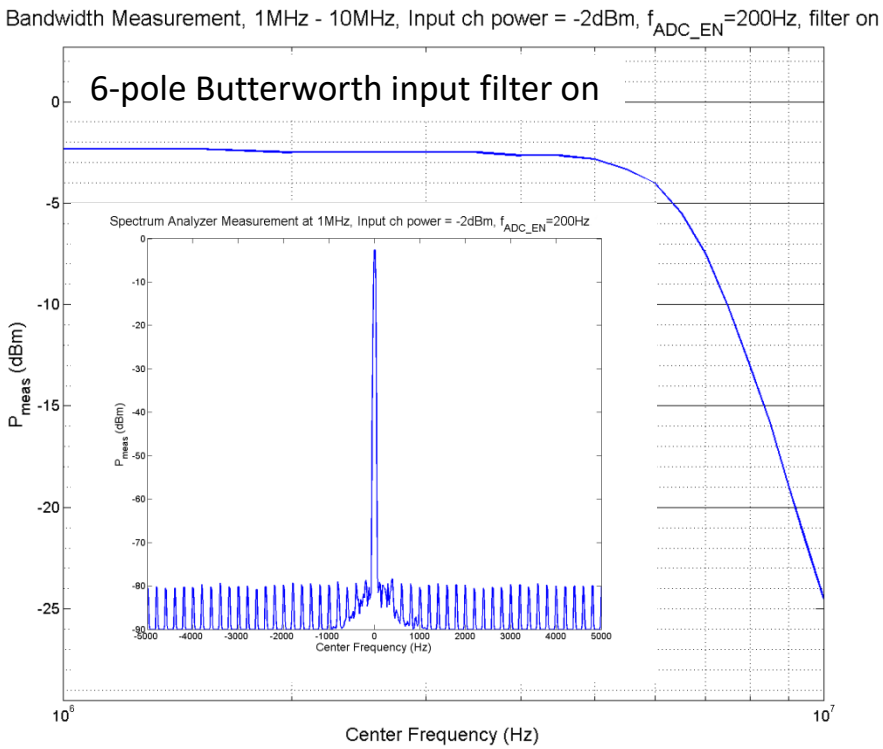
- On power-up the ICA chip loads an internal, default, diagonal weight matrix
- Each analog channel receives maximally weighted diagonal weight, with sign-bit=1. This means that a channel's output is an inverted version of it's input
- Analog signals passing through the ICA chip can be measured if EN_ADC reset is pulsed from Hi = 1 V to Lo = 0 V as shown in the following diagram
- EN_ADC evaluation time of between 1 and 5 milli-seconds, which is governed by the drift of the dc-operating point established during the reset-phase of the switched capacitor circuit implementing the multiplier.
- EN_ADC rise and fall times between 1 ns and 10 ns.
- EN_ADC reset time between 0.5 us and 1 us.

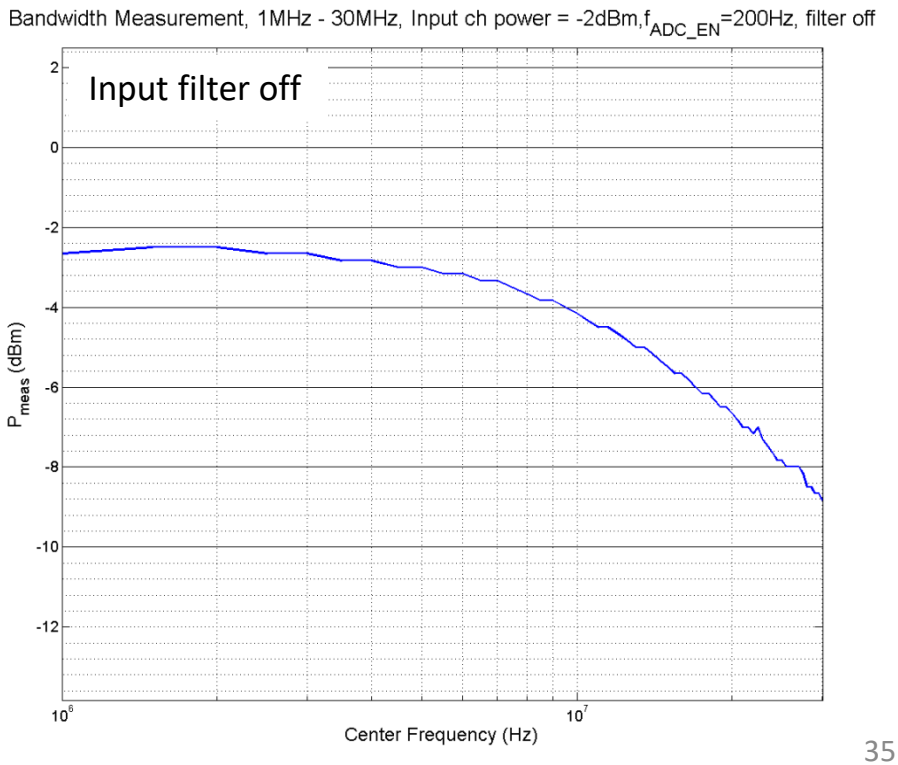


Initial analog tests

Channel 3 insertion loss
-3 dB at 6.5 MHz with input filter on (frequency sweep from 1 MHz to 10 MHz)
-3 dB at 15.4 MHz with input filter off (frequency sweep from 1 MHz to 30 MHz)

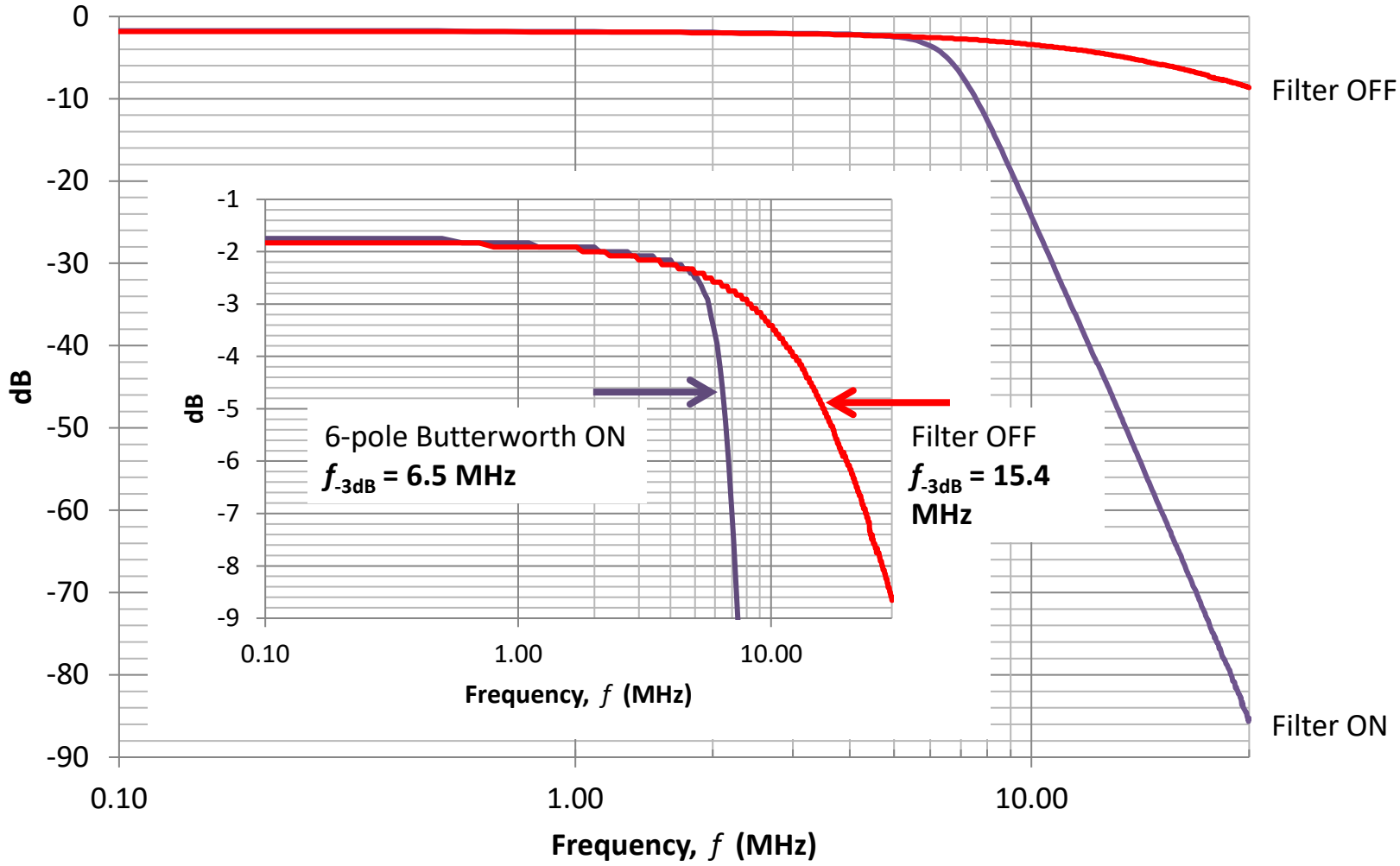
Configuration: input-board+**ICA-board**+output-board
-2 dBm input, EN_ADC has Hi=1 V, Lo=0 V, 200 Hz, 0.7 us pulse width Lo, 8.4 ns rise and fall



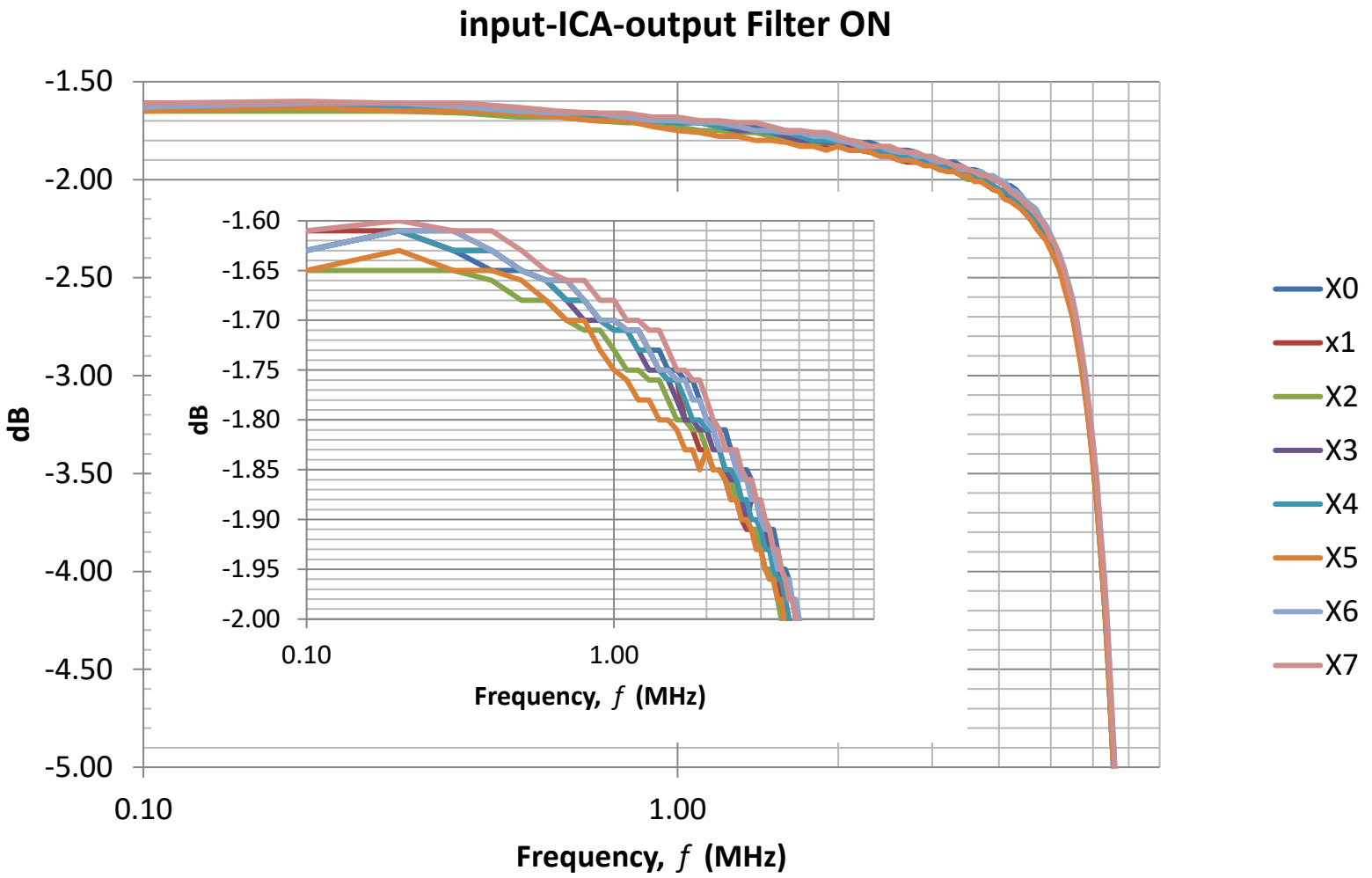


Initial analog tests

- Channel 3 insertion loss over frequency range 0.1 MHz – 30 MHz
  - f_{-3dB} **= 6.5 MHz with** 6-pole Butterworth ON
  - f_{-3dB} **= 15.4 MHz** with filter OFF
- Configuration: input-board+**ICA-board**+output-board
- -2 dBm input, EN_ADC has Hi=1 V, Lo=0 V, 1 kHz, 0.7us pulse width Lo, 8.4 ns rise and fall



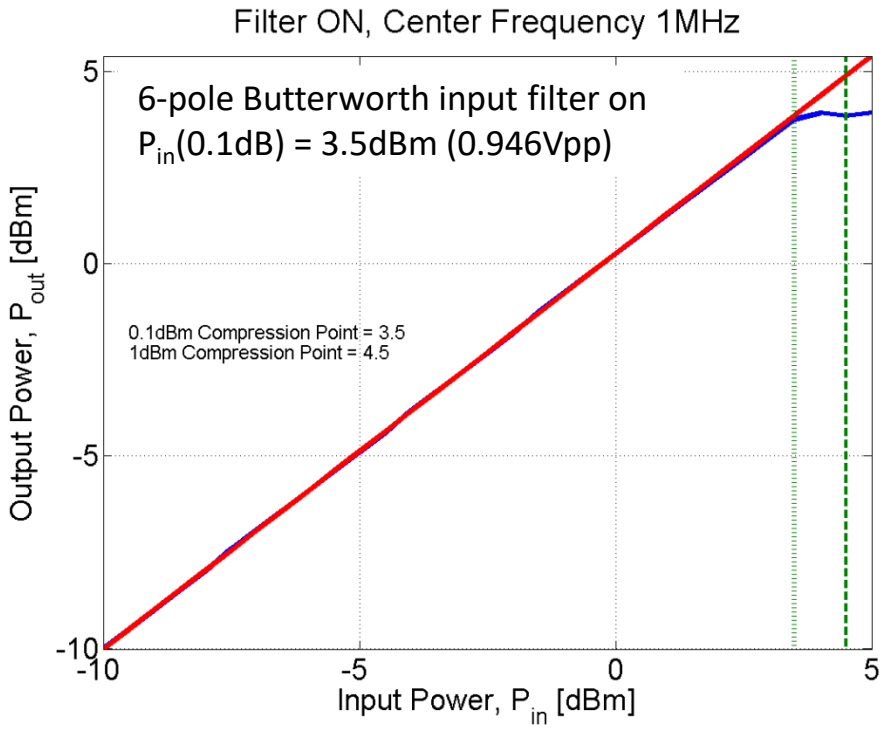
Initial analog filter gain matching, <0.7% uncalibrated

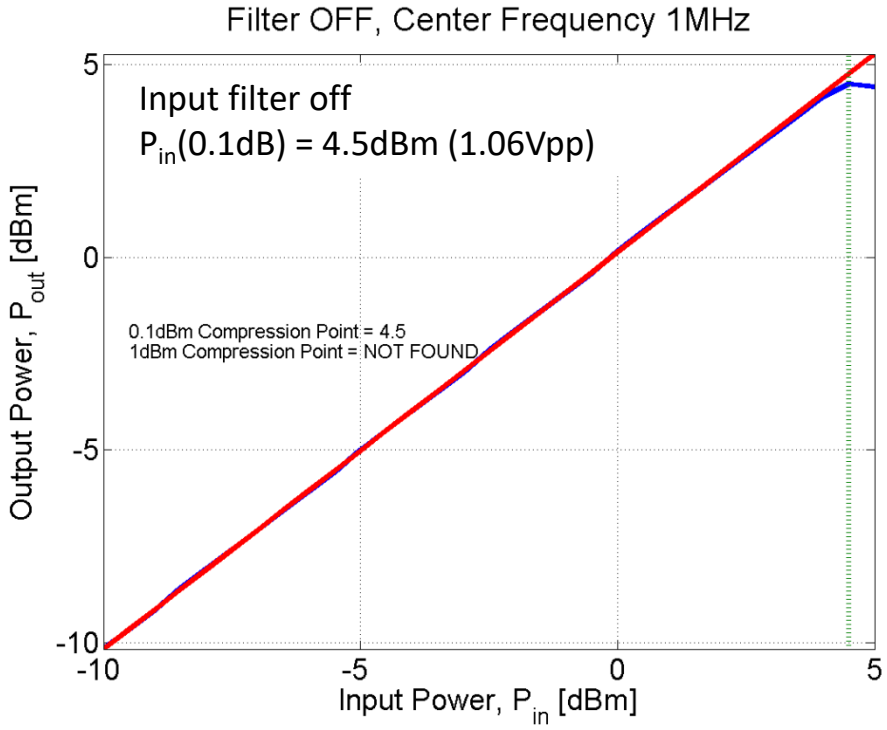


Configuration: input-board+**ICA-board**+output-board
-3 dB at 6.5 MHz with 6-pole Butterworth input filter on (frequency sweep from 0.1 MHz to 7.0 MHz)
Filter matching +/- σ = +/- 0.0291 dB (+/- **0.67%**) 0.1MHz – 7MHz and +/- σ = +/- 0.0198 dB (+/- **0.46%**) 0.1MHz – 2MHz
-2 dBm input, EN_ADC has Hi=1V, Lo=0V, 1 kHz, 0.7 us pulse width Lo, 8.4 ns rise and fall
Note: Close to measurement instrument resolution 0.01dB

Initial analog tests

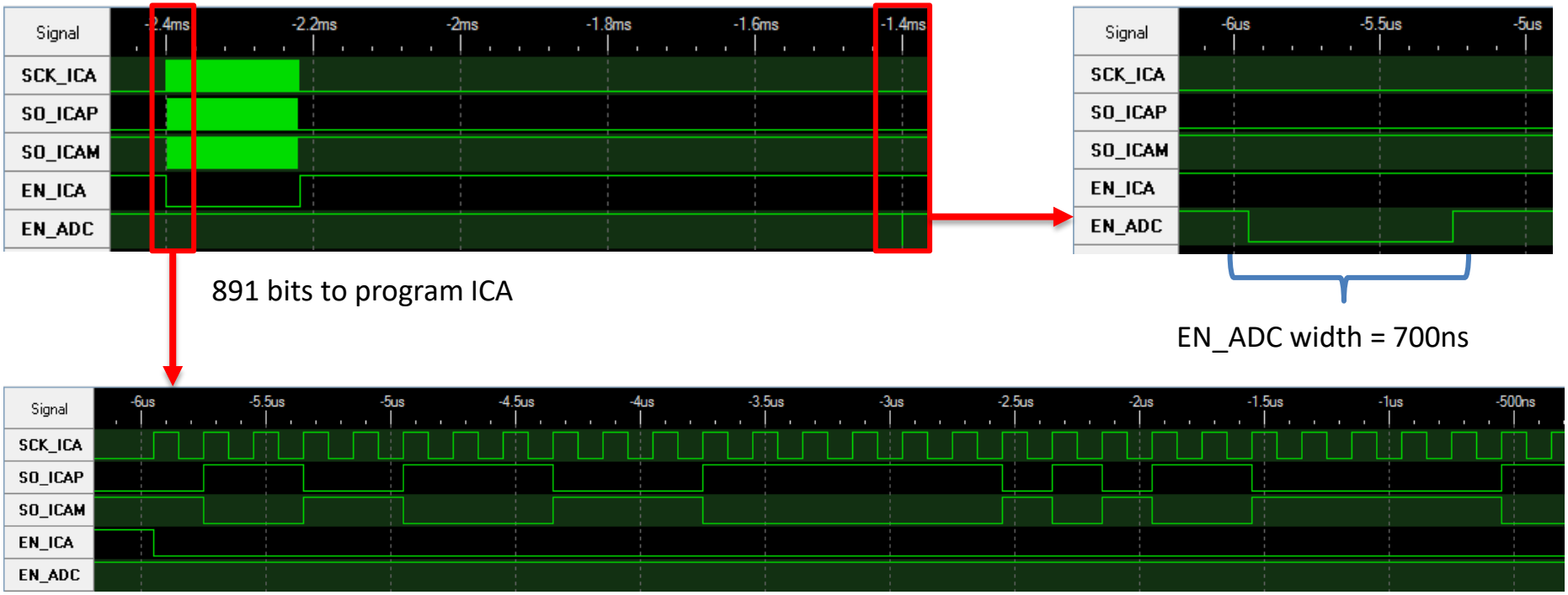
Channel 3 compression
0.1 dB compression at 1 MHz occurs at input power 3.5 dBm with input filter on
0.1 dB compression at 1 MHz occurs at input power 4.5 dBm with input filter off
Configuration: input-board+**ICA-board**+output-board
EN_ADC has Hi=1 V, Lo=0 V, 200 Hz, 0.7 us pulse width Lo, 8.4 ns rise and fall





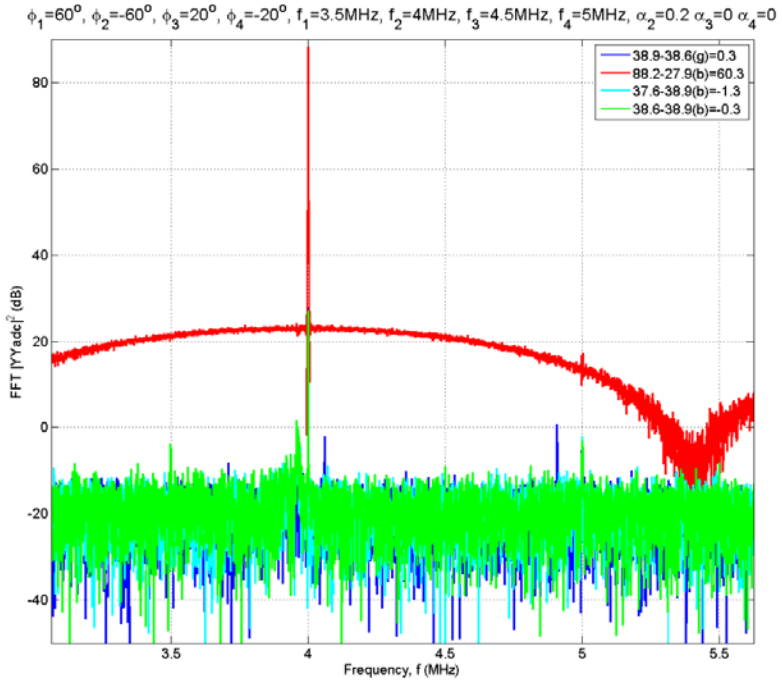
ICA programming

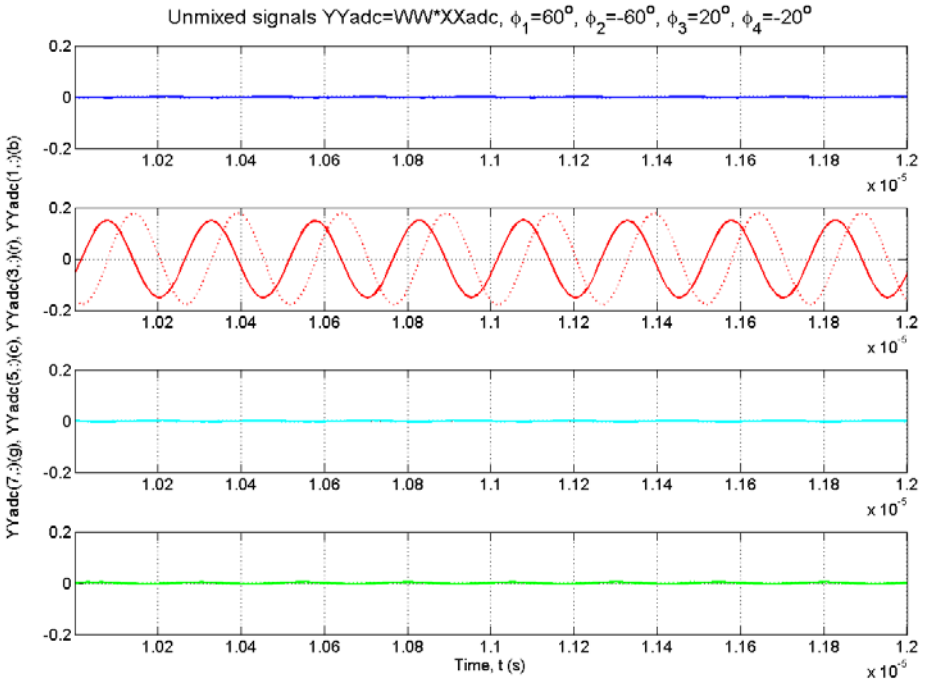
- Confirmed programming at 250 MHz ICA Clock Frequency (SCK_ICA)
  - 891 bits programmed in 3.564us
- Most initial experiments performed using 5 MHz clock
- SO_ICAP and SO_ICAM are the differential digital outputs of ICA data (891 bits)
- Data is shifted in when EN_ICA is low
- ICA serial-data is effected after the first EN_ADC that occurs after EN_ICA goes high



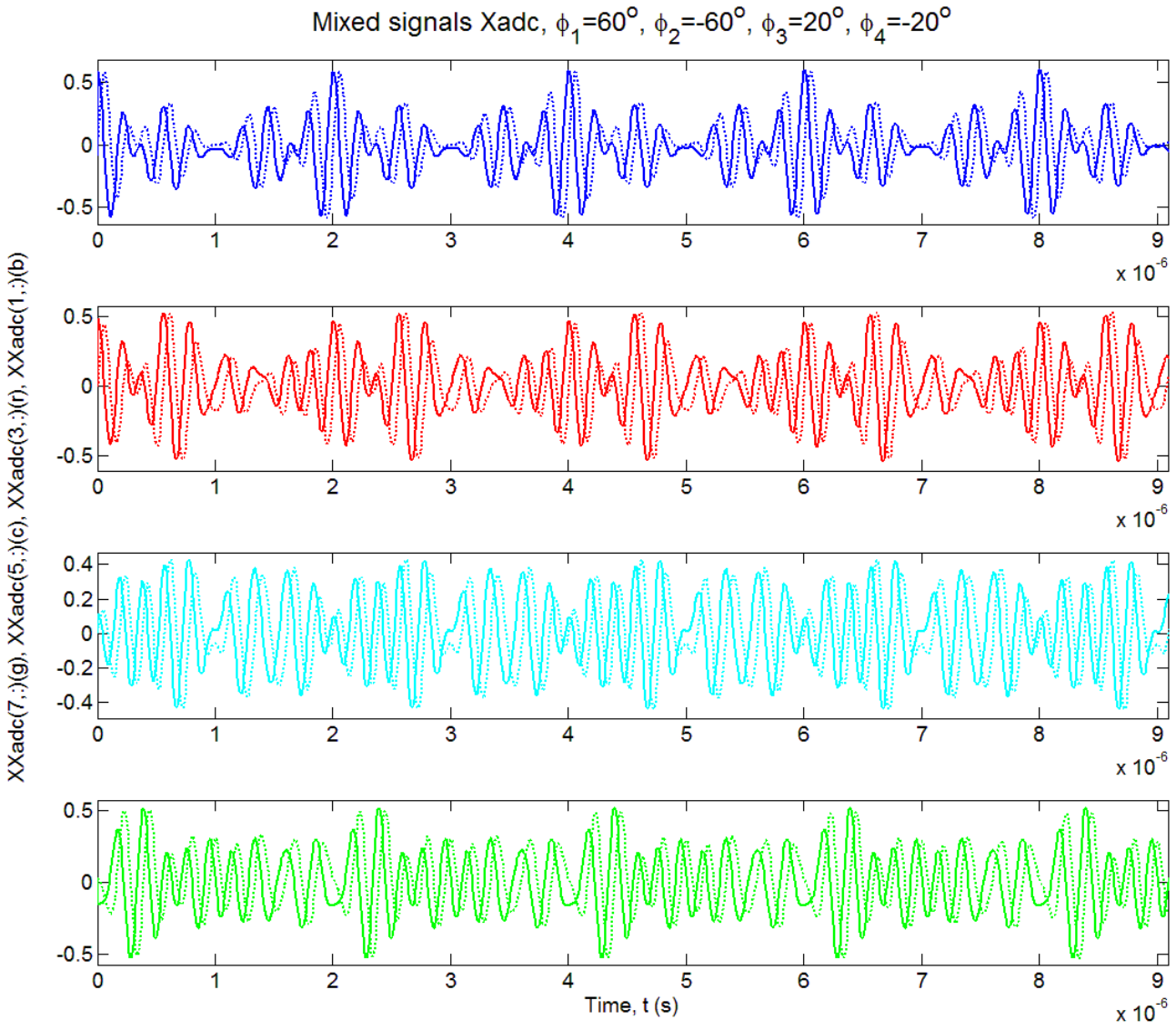
Initial Test 9 measurement, 4 antennas, unmixing single tone

- ICA matrix weights are for the Test 9 configuration at frequencies 3.5 MHz, 4.0 MHz, 4.5 MHz and 5.0 MHz and phase angles +/- 60^o and +/- 20^o
- 60.3 dB suppression in unmixed spectrum measurement of single tone at 4.0 MHz with 18 dB of output gain
- Noise background is from unfiltered EN_ADC switching
  - EN_ADC has Hi=1 V, Lo=0 V, 200 Hz, 0.7 us pulse width Lo, 8.4 ns rise and fall



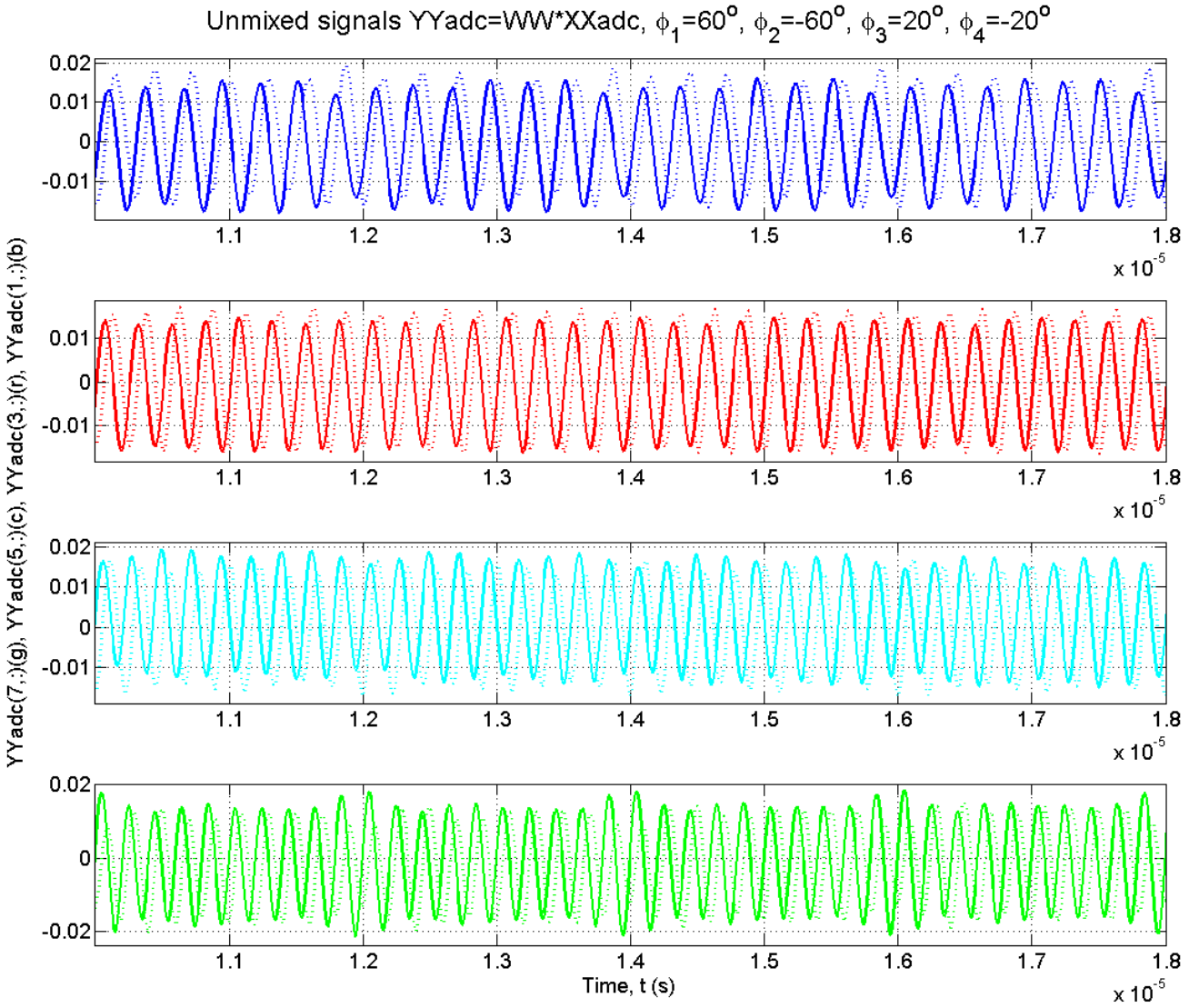


Initial Test 9 measurement, 4 antennas, 4 tones mixed signals

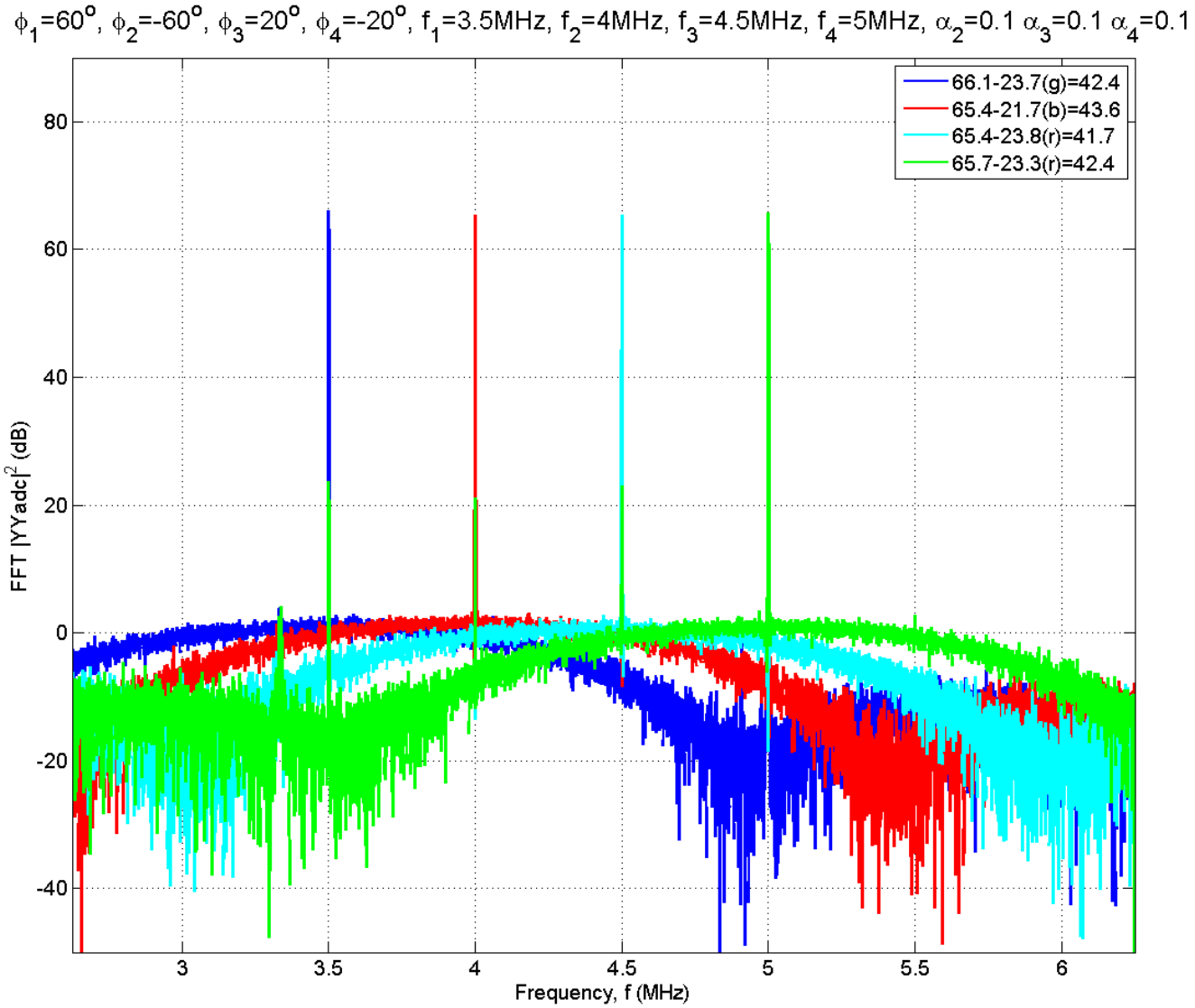


Frequencies, f_1 = 3.5MHz, f_2 = 4.0MHz, f_3 = 4.5MHz and f_4 = 5.0MHz

Initial Test 9 measurement, 4 antennas, 4 tones unmixed signals

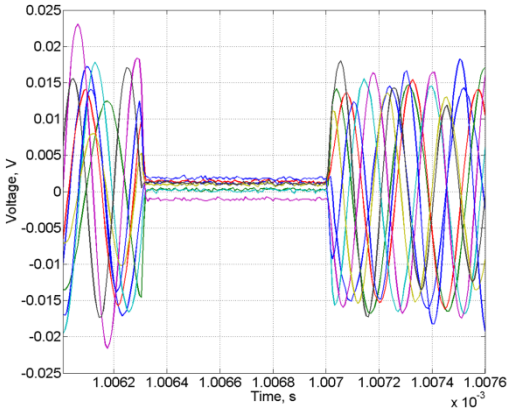


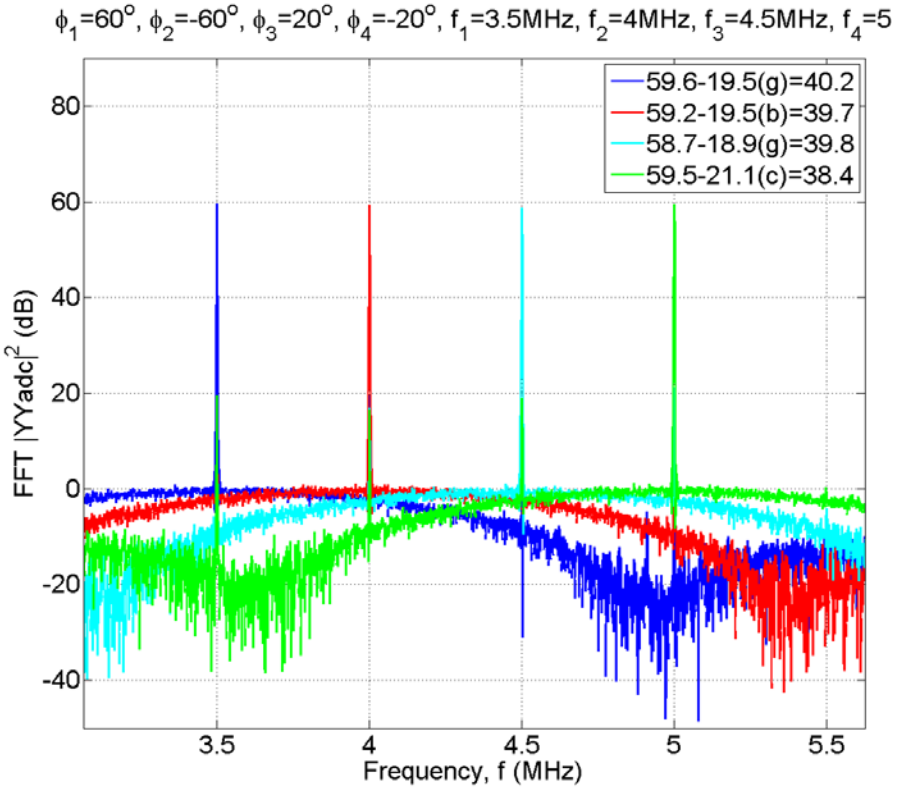
Initial Test 9 measurement, 4 antennas, 4 tones unmixed signals

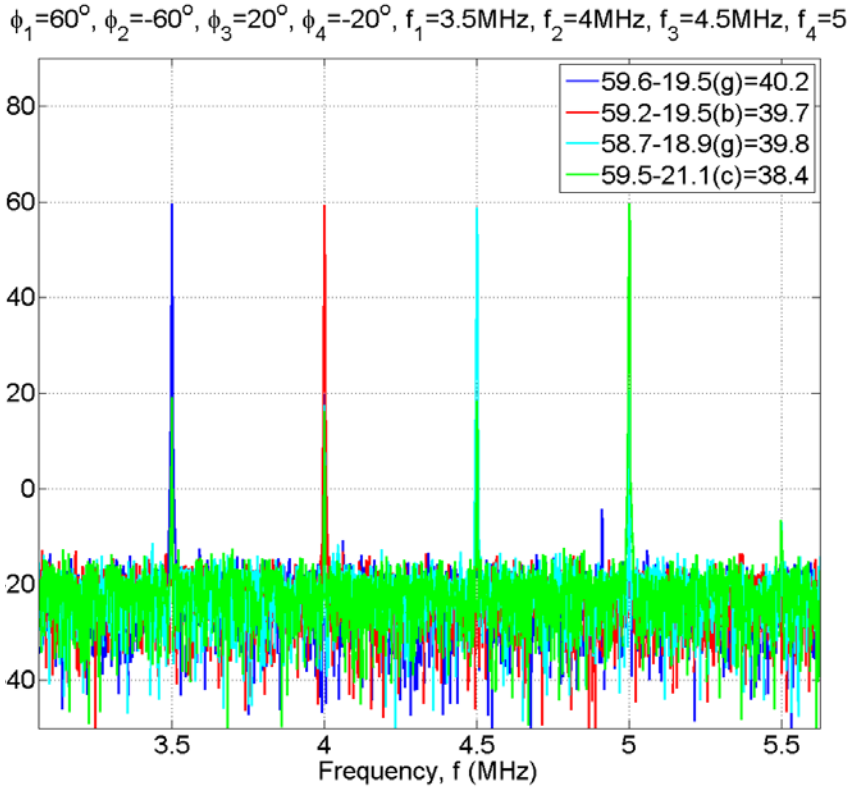


Removal of noise from EN_ADC reset signal

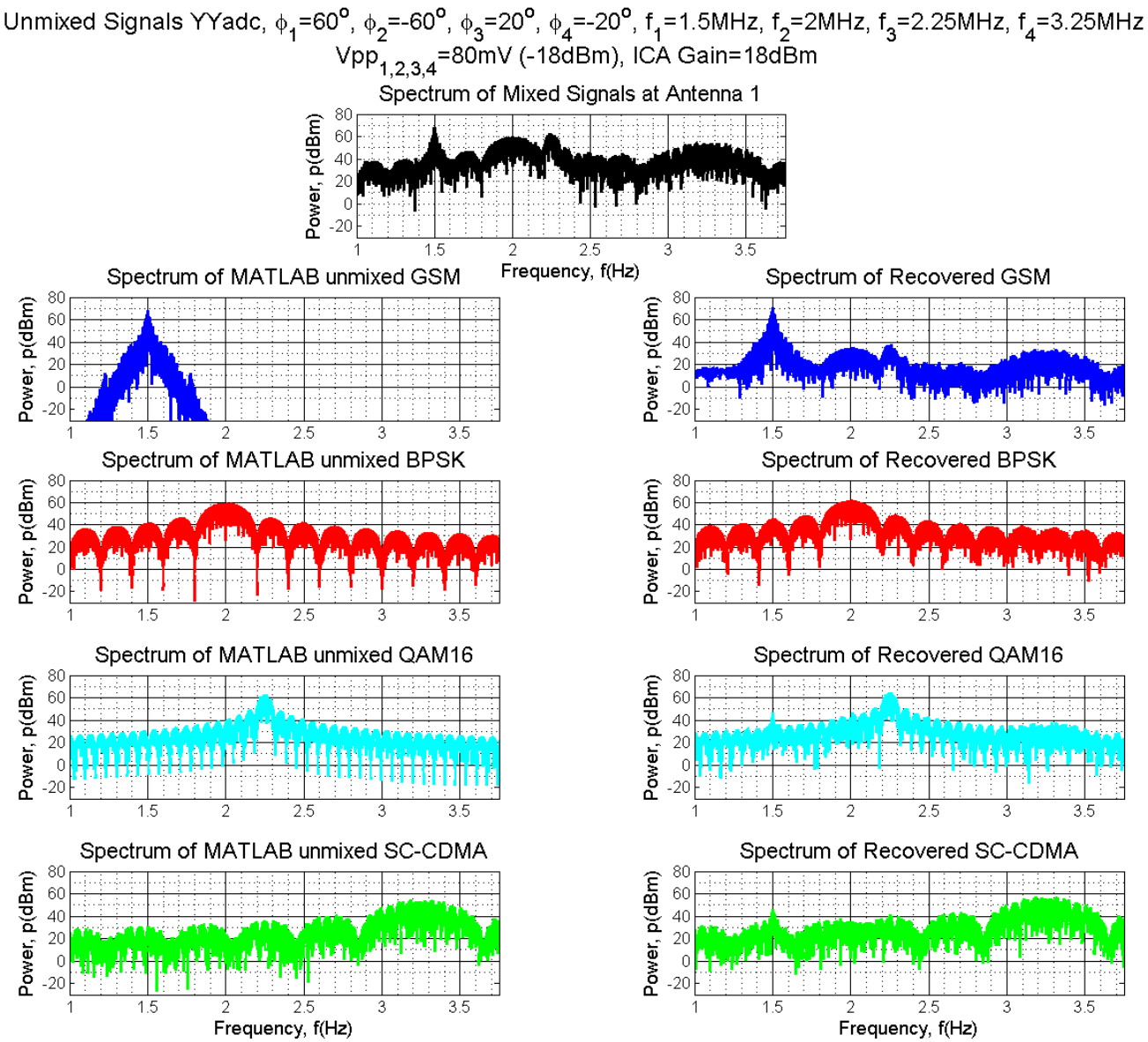
- As much as 20 dB noise background is from unfiltered EN_ADC switching that can be removed in time-domain before calculation of spectrum using windowed FFT
- EN_ADC has Hi=1 V, Lo=0 V, 200 Hz, 0.7 us pulse width Lo, 8.4 ns rise and fall



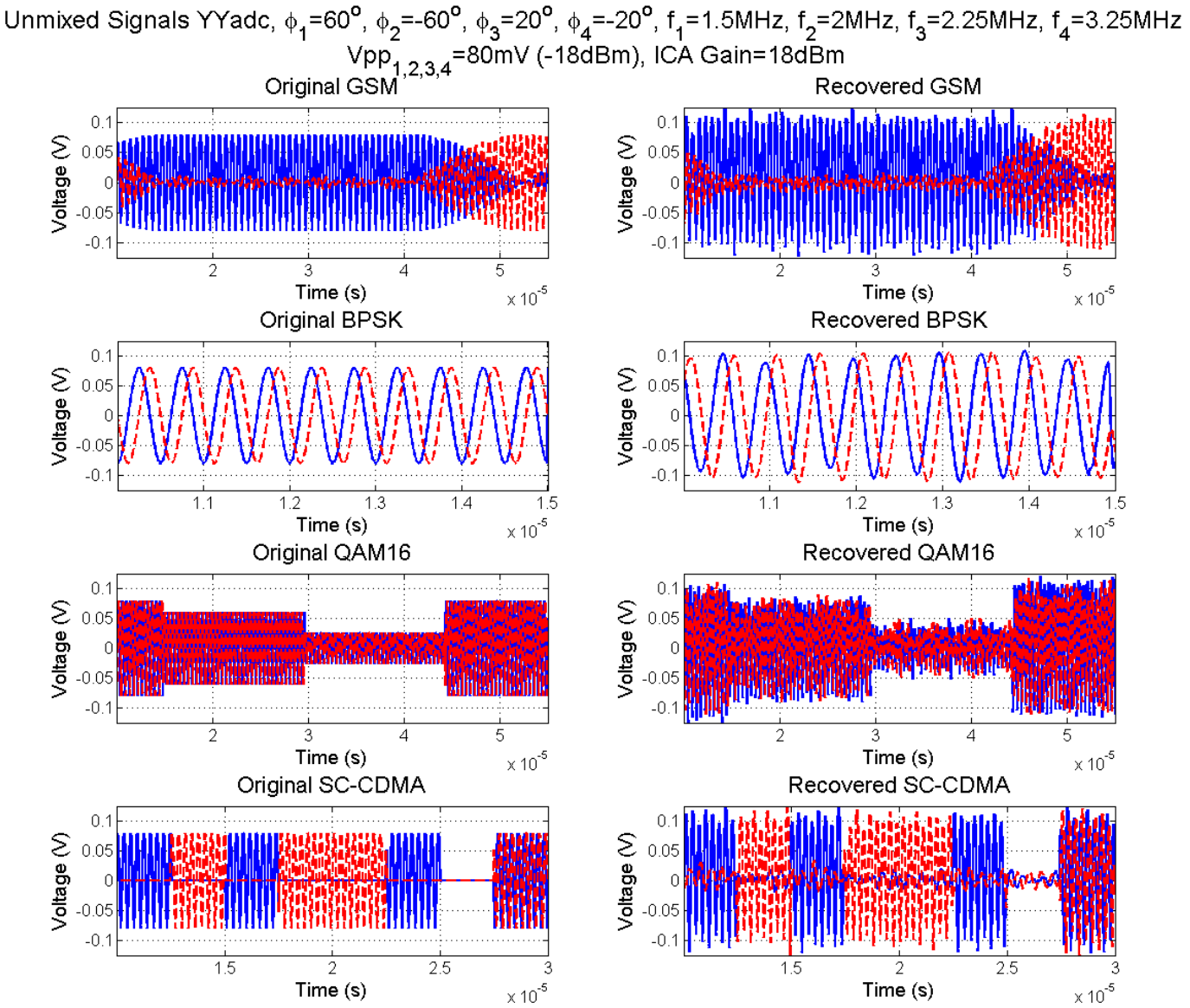




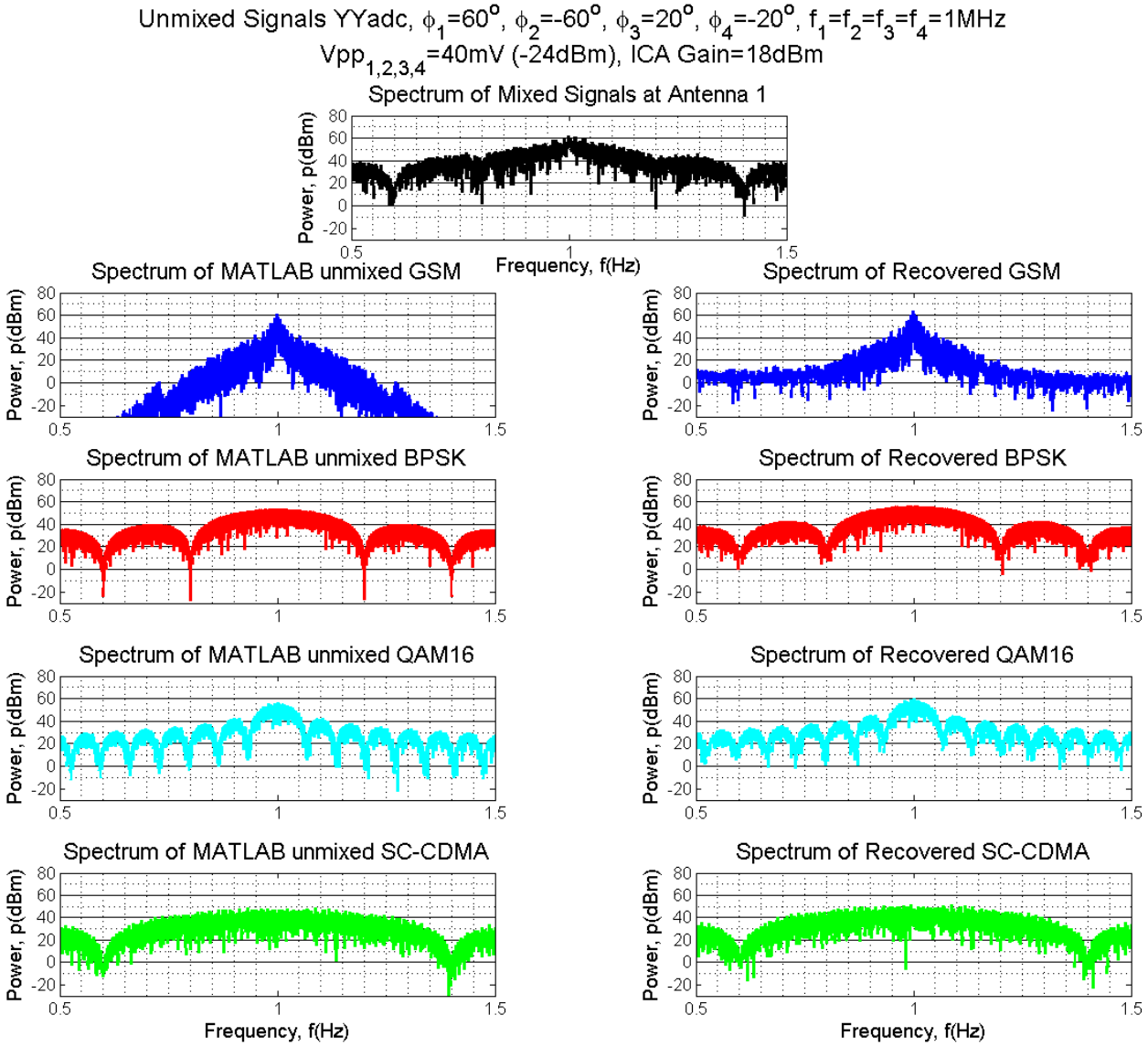
Test 9 measurement, 4 antennas, 4 communication waveforms with *different* center frequencies



Test 9 measurement, 4 antennas, 4 communication waveforms with *different* center frequencies

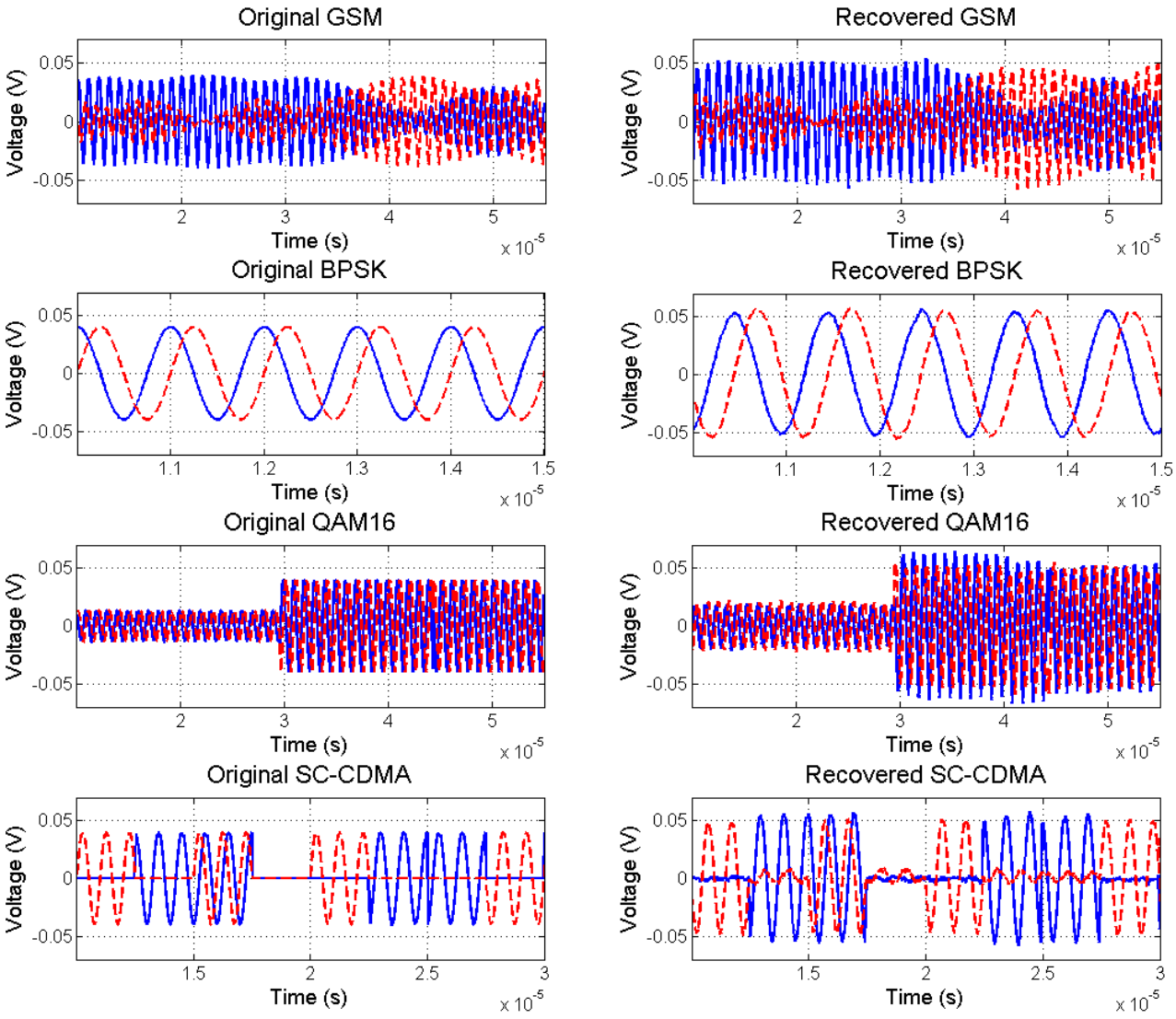


Test 9 measurement, 4 antennas, 4 communication waveforms with *same* center frequency (overlapping spectra)



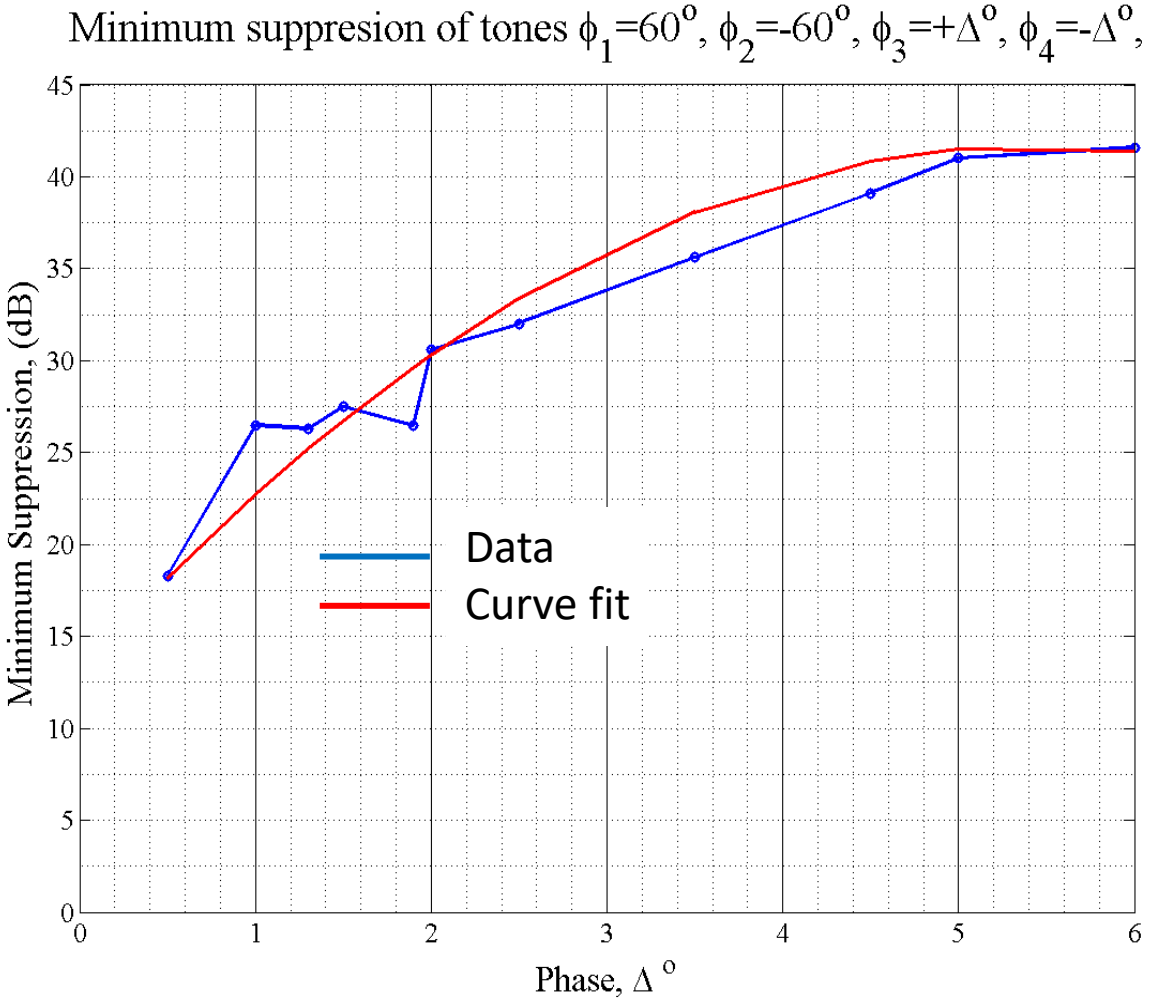
Test 9 measurement, 4 antennas, 4 communication waveforms with same center frequency

Unmixed Signals YYadc, ϕ_1=60°, ϕ_2=-60°, ϕ_3=20°, ϕ_4=-20°, f_1=f_2=f_3=f_4=1MHz
$Vpp_{1,2,3,4}$=40mV (-24dBm), ICA Gain=18dBm



4 antennas, 4 tones, minimum suppression ratio as function of phase angle, +/- Δ^o

- Motivation for testing using small phase angles, ϕ, is the relationship between angle of arrival θ, separation between adjacent antennas *L*, and baseband frequency *f* is ϕ = 1.2 x *f*(MHz) x *L*(m) x sin(θ). Assuming *f* = 10 MHz and a typical tablet device with *L* = 0.2 m (8 inches), then ϕ scales to +/- 2.4 .
- ICA matrix weights are for frequencies 1.5 MHz, 2.0 MHz, 2.5 MHz and 3.0 MHz and phase angles +/- 60^o and +/- Δ^o
- Measure 18 dB suppression at Δ=0.5^o with or without 18 dB of output gain



Design and measured accomplishments of 8-channel ICA test chip

Criterion	Requirement	Design result	Measured
Gain matching	+/- 3% across PVT	Designed to better than +/-3% across PVT without calibration	Better than +/- 0.7%
Channel (LPF+ICA+Driver) BW	6.5 MHz across PVT	Design meets specification	LPF 6.5 MHz
Channel (LPF+ICA+Driver) linearity	Better than 63dB across PVT per two-tone test	Design meets specification. 68.19dB at TT/27C/1.2V	68 dB
ICA weights	13b (sign bit +12 magnitude bits)	Design meets specification	
ICA weight monotonicity	Guaranteed monotonic	Design meets specification.	
Maximum input signal	1 Vpp	Design meets specification	0.1 dB compression
Input referred noise	< 300uVrms	288uVrms	430 uVrms including input and output boards
1b ADC sampling rate	125 MS/s	Design meets specification. 8b DAC threshold mismatch is within 1%	
ICA weight update rate	Max. 100 kHz	Design meets specification	Programming 250 MHz
1b ADC 8-b DAC update rate	Max. 500 kHz	Design meets specification	

PVT is all process corners, 1.2V +/- 5%, -55°C to 125°C junction temperature

Summary

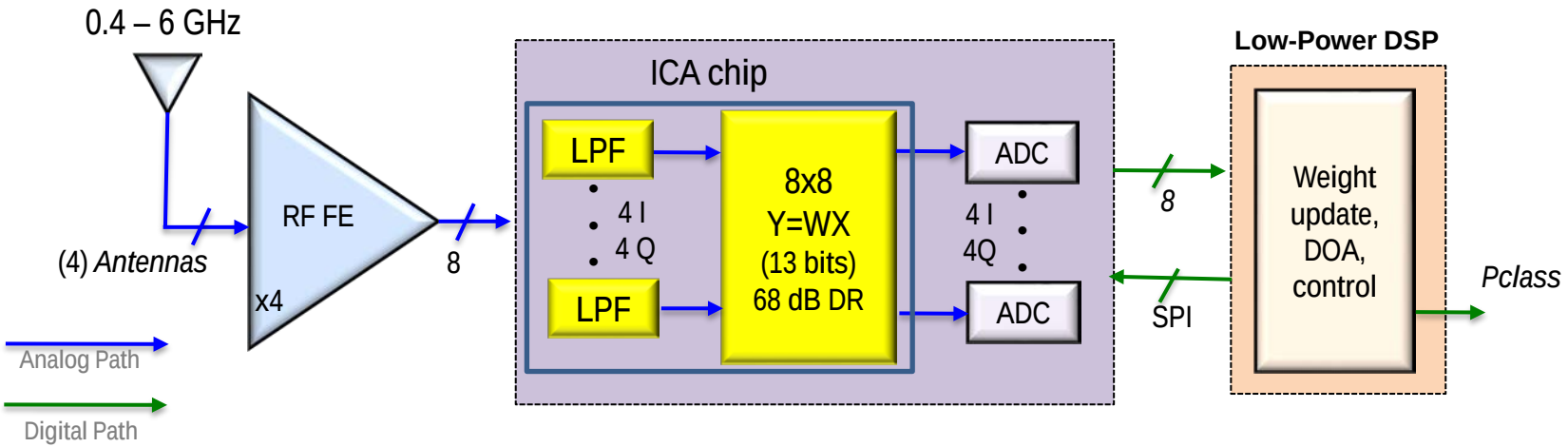
- Successful initial laboratory test and validation of basic closed-loop functionality of ICA chip implemented in GF65LPE (3.8 mm x 5.5 mm)
- Real-time 8 input, 8 output, programmable 8 x 8 matrix multiply to un-mix 4 complex IQ baseband signals
  - 64 matrix elements, each digitally programmable to 13-b in total time of 3.328 us at 250 Mb/s and with 100 kHz update rate
  - Complex ICA can be performed on 4 antenna signals with >40 dB suppression between unmixed signals
- Overall 68 dB chip linearity (11b) with no calibration and $f_{\text{-3dB}}$ = 15.4 MHz bandwidth per channel
  - $f_{\text{-3dB}}$ = 30.8 MHz I-Q bandwidth per antenna
  - 0.1 dB compression at 1 MHz occurs at input power 4.5 dBm (1.06 Vpp)
  - Core ICA function is 0.7 nJ/MAC
- On-chip selectable 6-pole low-pass Butterworth input filter with $f_{\text{-3dB}}$ = 6.5 MHz and gain 0.7% matching with no calibration
- On-chip selectable 125 MS/s 1-b ADC with 8b DAC reference level programed in 0.256us at 250 Mb/s and with 500 kHz update rate

Team

- USC
  - USC lead: Tony Levi
  - Mixed signal circuit design: Bindu Madhavan and Edward Lee
  - Testbed: Joshua Zusman
- SAIC/Leidos
  - SAIC (Leidos) lead: Dennis Braunreiter (Douglas Miller)
  - Algorithm development: Don Finnel (James Sifferlen)

Backup

System architecture



- Integrated selectable oversampled 1-bit ADC with programmable 8-bit DAC for threshold and selectable LPF
  - 1-bit ICA processing
    - ICA algorithm and gain adjustment
  - Direction of arrival (DOA) algorithms
  - Basic tracking algorithms
  - 15 MHz BW, 60 dB dynamic range, 13 bit programmable matrix weights
  - Selectable off-chip ADC and LPF bypass

Conventional digital receiver processing versus ICA chip

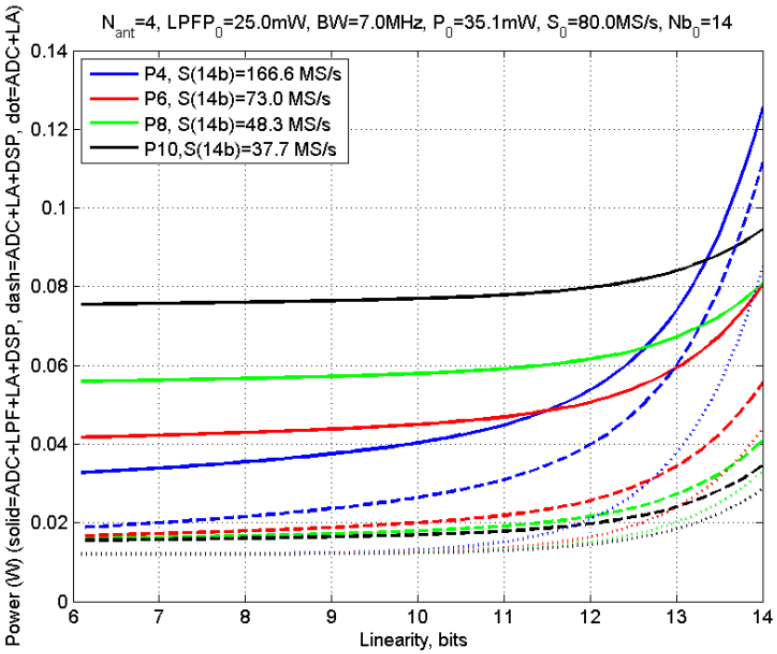
Scaling about the reference point in 65nm CMOS

ADC power scaling linear with sample rate using interleaving to increase 1-bit is 2x power plus 20% premium for calibration
- Analog Devices research 14b, 80MS/s, 35.1mW (with ref) in 65nm CMOS, ISSCC 2013

LPF power increases linearly with number of poles and 20% premium for matching and calibration per pole
- 6-pole LPF, 0.5dB ripple, 25mW in 65nm CMOS

DSP requires Nop with Jop (J/op) at the sample rate
- DSP 10pJ/op

LA (linear amplifier) power is fixed in BW and dynamic range
- 86dB linearity, 12mW in 65nm CMOS



Digital receiver replacing the ICA function (<1mW with additional design time) with 10-11b dynamic range and 20dB SNR on minimum signal requires:

ADC (14b, 73MS/s), 6-pole LPF, LA, DSP = 80mW (note 6-pole LPF is power optimum for this case!)

Compared to CLASIC ICA, 6-pole LPF, 8b ADC = <1mW+25+0=<26mW (we only need 8b(85uW) to 10b (<0.6mW) ADC because signals are separated by ICA)

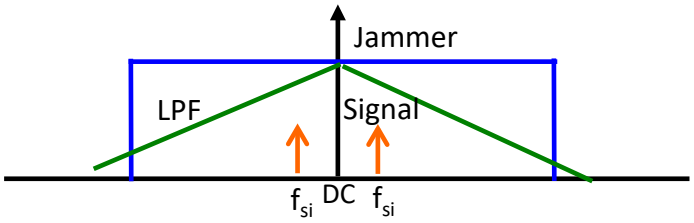
Because the LPF is common it could be factored out in the comparison, in which case:
Digital receiver ADC (14b, 73MS/s, 32.02mW), LA (12mW), DSP (11.68mW) = **55mW**

Compared to CLASIC ICA (<1mW with additional design time), 8b ADC (85uW) = <1mW + 85u = **1mW** giving approximate **ratio 55**

Why ICA in analog? Low power small signal demodulation against jamming

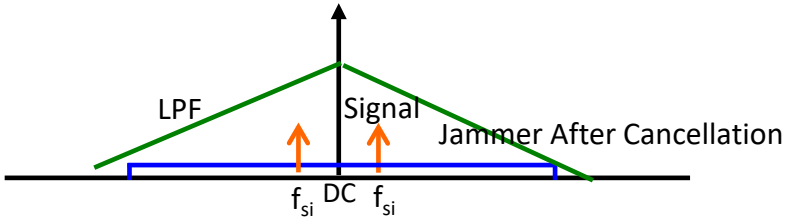
- Conventional Digital Receivers (CDR) susceptible to jammer interference
  - Sum of all received signals MUST be digitized first
  - Blocking of jammer signal can only occur AFTER the ADC
- The ICA chip spatially blocks jammers BEFORE the ADC
  - Allows much relaxed ADC specification
  - Minimum signal output SNR (circuit) = 20 dB
- Jammer EXAMPLE **5-6 bit Savings**:
  - ICA chip linearity is >10-b (11-b) over 10 MHz
  - Resolving small signal and jammer requires CDR to have 10-b linearity for ICA function, plus 20dB = 3-b SNR for demodulation
  - CDR LPF must be sampled at higher rates than Nyquist to prevent aliasing of interference OR additional bits to reject aliased jammer
    - Filter attenuation = -120 dB/decade (6 pole filter) -> 24 dB attenuation at Nyquist
    - Jammer sampled at Nyquist folds over additional aliased signal power on top of small signal
    - Need 1-2 additional bits to resolve small signal for higher power jammer

Continuous Spectrum Before Sampling

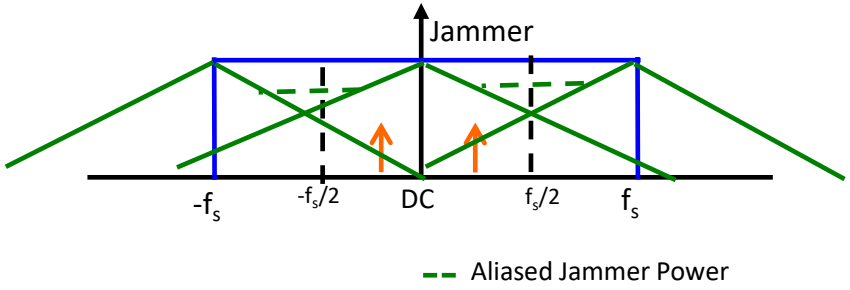


f_{si} = signal frequency

Continuous Spectrum After ICA chip

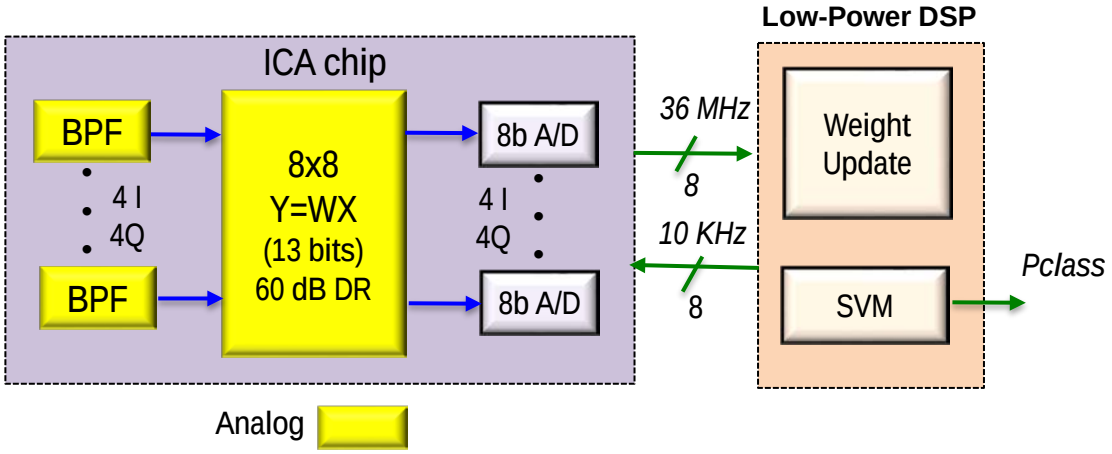


CDR Spectrum After Sampling



DSP Requirements

- DSP algorithms performed on low power digital hardware
- Required processing
  - Weight update to ICA
  - Direction of arrival DOA calculation
- Weight update processing rate = 10 kHz (100kHz possible)
- ~10 mW



Ultra low power DSP TI part TMSC320C5534

	Weight Update	DOA
Additions	257	80
Multiplies	1027	192
MACs	1728	0
Divisions	2	12
Miscellaneous	83	0
Total Operations	3097	284
Target Processor Efficiency	50	50
Update Period (microseconds)	100	1000
Millions of Ops Per Second	61.94	0.568
Desired Processor Clock Rate	**62.508**	

~10 mW

Power is .15 mW per MHz requiring at least 50% efficiency in processing

Design accomplishments of 8-channel ICA test chip

Criterion	Requirement	Design result
Input LPF out-of-band supression	50-dB	**-50dB BW between 12MHz and 26MHz across PVT.**
Gain Matching	+/- 3% across PVT.	**Designed to better than +/-3% across PVT without calibration.**
BW Matching	+/- 3% across PVT.	**Designed to better than +/-3% across PVT without calibration.**
Channel (LPF+ICA+Driver) BW	at least 4.6875MHz across PVT. Allowed to vary +/- 30% across PVT while maintaining matching.	**Design meets specification. BW between 4.73MHz (SSF/Rmax/Cmax/125C/1.13V) and 10.17MHz (SSF/Rmin/Cmin/-40C/1.26V).**
Channel (LPF+ICA+Driver) linearity	Better than 63dB across PVT per two-tone test.	**Design meets specification. 68.19dB at TT/27C/1.2V, worst case is 63.39dB at SSF/Rmax/Cmax/-55C/1.13V).**
ICA weights	13-bit (sign bit+ 12-magnitude bits)	**Design meets specification**
ICA weight monotonicity	Guaranteed monotonic	**Design meets specification**
ICA weight matching	+/- 3% across PVT.	**Designed to better than +/-3% across PVT without calibration.**
Maximum input signal	1Vp-p	**Design meets specification**
Minimum input signal	1mVp-p	**Design meets specification**
Input-referred noise	<= 300μVrms	**288.1μVrms at TT/27C/1.2V**. Exceeds target by being between 353.4μVrms and 373.8μVrms at 125C in eight (8) out of total 39 corners. **Occurs only 1:10M.**
1-b ADC sampling rate	125 MHz	**Design meets specification. 8-bit DAC threshold mismatch is within +/-1% across PVT. 1-bit comparator simulated with 0.5V to 0.9mV differential input pattern sampled at 125MHz passes MC.with DAC at min and max.**
ICA weight and 1-bit ADC 8-bit DAC update settling time	< 0.5μs	**Design meets specification**
ICA weight update rate	maximum 100 kHz	**Design meets specification**
1-b ADC 8-bit DAC update rate	maximum 500 kHz	**Design meets specification**

PVT is all process corners, 1.2V +/- 5%, -55°C to 125°C junction temperature

Bring up

Input board:
+3.3 V (0.32 A when not connected, 0.45 A when connected to ICA board)
- 1.7 V (0.28 A when not connected, 0.24 A when connected to ICA board)

ICA board:
Power up analog voltage first followed by digital
+1.2 V analog (0.26 A [312 mW] filter OFF, 0.42 A [504 mW] with filter ON)
+1.2 V digital (0 A)

Output board:
+5V (0.14 A)
- 5V (0.14 A)