Single-Electron Memory for Giga-to-Tera Bit Storage

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Invited Paper

Starting with a brief review on the single-electron memory and its significance among various single-electron devices, this paper addresses the key issues which one inevitably encounters when one tries to achieve giga-to-tera bit memory integration. Among the issues discussed are: room-temperature operation; memory-cell architecture; sensing scheme; cell-design guideline; use of nanocrystalline silicon versus lithography; array architecture; device-to-device variations; read/write error rate; and CMOS/single-electron-memory hybrid integration and its positioning among various memory architectures.

***Keywords*—** *Coulomb blockade, MOS memory integrated circuits, quantum dots, quantum effect, semiconductor devices, silicon, single-electron devices, very large scale integration.*

I. INTRODUCTION

Single-electron devices, in which the addition or subtraction of a small number of electrons to/from an electrode can be controlled with one-electron precision by using the charging effect, have recently attracted much attention [1]–[3]. The operation of single-electron transistors [4]–[6], the transfer of a single electron [7], [8], and memory operation with a small number of stored electrons [9]–[15] have all been demonstrated. These are interesting not only as new physical phenomena in nanostructures [16] but also because they offer new operating principles for future integrated-circuit devices [17], [18].

The advantages of the single-electron devices are as follows. Good scalability is the strong incentive to explore the possibility of this device. Because the operating principle relies simply on the Coulomb repulsion among electrons, single-electron devices are anticipated to operate even with very small physical dimensions, such as atomic scale, making ultralarge scale integration possible. Another advantage is its ultralow power operation, simply because they use very small number of electrons to accomplish basic operations. Another advantage may be faster operation. In conventional devices, more than 100 000 electrons are charged/discharged for a basic digital operation. In single-electron devices, only a few electrons are transferred, therefore, the process might be faster than those of conventional devices.

Sometimes the terminology a "single-electron device" confuses the discussion, so the definition is clarified here. Although the name makes it sound like the device works only with one electron, this is not in any sense true. Even a single atom contains a number of electrons and a metal- or semiconductor-based "single-electron" device should have huge number of electrons which have relevance to the operation. Another narrow definition may be "a single-electron device or circuit should use addition or subtraction of one electron to/from an electrode to represent a digital bit." This excludes most of the interesting effects arising from Coulomb blockade, which include Coulomb oscillation, Coulomb staircase, turnstile operation, except the lowest peak/plateau related to the one-electron transfer, so it is too narrow. A more sound definition, which is consistent with the use in the literature in the field, is that "a single-electron device utilizes one-electron-precision charge transfer based on the Coulomb blockade effect for its operation." With this definition, the above operation of a wide variety of single-electron devices/effects are covered. The number of electrons, in this definition, transferred between electrodes might be 100 or even 1000 in a single-electron device, but within one-electron precision, although a better control of the electron count naturally invites the use of smaller number of electrons in the operation.

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Among a variety of proposed single-electron devices, the single-electron memory, we believe, has the special importance in the light of use in large scale integrated (LSI) circuits. There are two reasons that we emphasize memory rather than logic. One attractive aspect is that we can use single-electron devices only in a memory cell, whereas we keep using conventional CMOS technology in the peripheral circuitry. Changing everything on the chip from the conventional technology to the new one is difficult in the sense of technology itself as well as economics and human factors. The above hybrid approach is a far more realistic scenario. If we look into what happened in the last ten years, memory-cell technology has continuously changed, including the emergence of flash memory technology and ferroelectric-film memory technology. This can be interpreted as the memory technology still having plenty of room with which to play, and innovations are strongly desired from the user side of storage needs. This aspect is further emphasized if we look at the fact that our way of storing information is rapidly changing from the older regime, relying on papers and other analog electronic means, to the digital regime in the multimedia era. This might create new needs of storing information being different from the older specifications in bandwidth, storage capacity, power consumption, and so on.

Another reason is the fundamental difficulty with the single-electron device when it is used in a logic functional unit. The communication with another distantly placed logic unit is a fundamental requirement for a logic device. However, the single-electron devices (generally) have poor current-drive capability and are far inferior in such communication capability as compared to conventional CMOS devices. Although no one can deny the possibility of future emergence of clever ideas to overcome this difficulty, it strongly limits the use of those devices in logic circuits. Another direction may be going beyond digital logic by exotic concepts such as in [19]–[21], [49], and [50], however, these researches are in such an early stage that we have to wait until an accurate evaluation can be made.

Recently, researches in this field have also been placing more emphasis on memory [22]–[24]. A variety of memory devices have been fabricated and successfully operated, some of them at room temperature. Looking back at the history in this field, the charge quantization in a single-electron box-like structure was investigated by Lambe and Jaklevic [25] in 1969. Although the research in the single-electron physics/device field became very active in mid-1980's after the introduction of the single-electron-transfer oscillation [26], [27] single-electron transistor [28] by Averin and Likharev, at that time the emphasis was placed on digital logic gate rather than memory [17]. After the experimental operation of single-electron transistors [4], [5], synchronous transfer of single-electrons became an active research subject [7], [8], [29], [30]. Although the purpose of these researches was to understand the dynamic behavior of single-electron transfers, they are related to memory operation. These devices create temporal single-electron charge-quantized states, although the retention time should be short and there were no means to directly read out the stored state. A device structure that can read out the stored charge states was made by Fulton *et al.* [9] and clear hysteresis curves were observed. However, the purpose of this work was to investigate the transfer phenomena through highly resistive junctions, not memory operation. The first device clearly aimed at single-electron memory operation was made and analyzed by Nakazato *et al.* [10]. The device had write, read, and retention functions using GaAs/AlGaAs structures, and the measured characteristics were confirmed to agree with Coulomb blockade model. Dresselhaus *et al.* [31] also demonstrated metal-based memory device based on Al/Al_2O_3 technology and obtained similar results.

All these experiments were conducted at very low temperatures. To understand in-depth physics, low-temperature operation is not a problem or may be desirable. However, to apply these devices in electronics, low-temperature operation strongly limits the range of applicable field, and the potential impact on the industry/society. However, room-temperature operation requires large Coulomb energy accomplished only with sub-10-nm structure, which is beyond the current lithography limitation.

To overcome this difficulty, various ideas have been devised. Single-electron phenomena were observed at room temperature by Shönenberger and van Houten [32]. They used a scanning tunneling microscope (STM) on a metal particle and observed Coulomb staircase in the current-voltage characteristics through the tip. Another room-temperature observation, which is related to the single-electron memory, is random-telegraph noise [33]. Trapping of electrons into the interface states has much in common with the single-electron memory. The first room-temperature memory device based on single-electron tunneling was operated by our group [13], [14]. Our idea was to use very thin poly-silicon, (we use the terminology nanocrystalline-silicon, or nano-Si, hereafter) in which nanostructures were naturally formed, making an abrupt surge of operating temperature to room temperature possible. Based on this structure, operation of single-electron transistor [34] and synchronous single-electron transfer device [35] at room temperature have been demonstrated.

This room-temperature memory demonstration included another new concept: highly charged sensitive one-transistor floating-dot memory-cell [13], [14], which has been the basis of subsequent device demonstrations by some groups. Tiwari *et al.* [22] have demonstrated the use of nano-Si particles to replace the floating gate of memory device. They showed encouraging results for better endurance and faster write than conventional floating-gate type memory devices. Nakajima *et al.* [23] and Guo *et al.* [24] independently developed a one-transistor floating-dot memory device, however in these devices the narrow channel and floating dot are controllably defined using lithography rather than using natural nanostructure.

Efforts to make stable room-temperature devices have continued. Takahashi *et al.* [37] used a thin silicon-on-insulator film and a special oxidation technique to inten-

tionally define the 10-nm scale structures and an operated room-temperature single-electron transistor. Matsumoto *et al.* [38] used STM to oxidize Ti isolating a metal-based dot. Room-temperature operation of single-electron transistors has been demonstrated. The possible advantage of using semiconductor barriers for high temperature operations are suggested in [14], [15], and [36].

More integrated-circuit-directed work has also been advanced rapidly. Our group has reported the first memory integrated circuit, a 64-bit memory array, at IEEE International Solid-State Circuits Conference (ISSCC) 1996 [15]. We not only demonstrated the memory array operation in this report, but we also evaluated reliability and device-to-device characteristics scattering data, which are an unfamiliar agenda for these novel devices. The first LSI circuit, a 128-Mb memory, was reported in ISSCC 1998 [39], [43]. In this report, the positioning of the single-electron memory chip is focused to be the minimum bit-cost technology, for which two-storied memory-cell structure with the memory-cell size of a quarter of a typical DRAM cell has been devised.

Device-to-device scattering has been the major concern for serious consideration of this device in electronics [1], [2], [40]. Just one background charge, e.g., a charged ion in the insulator, might drastically affect the electrical property of those devices as suggested by Averin and Likharev [1], [2]. Also, process-related variations cannot be avoided in the real devices. As for floating-dot one-transistor memory devices, one can improve the operation margin by simply increasing the target number of stored electrons. More tight control has been demonstrated by the use of verify operation [41], in which the completion of the write operation is checked by reading out the data. Iterative sequence of readout and rewrite dramatically improves the various scatterings. In a metal-dot system, controlling background charge seems to be more difficult because the above simple increase of the target electron count does not help under the oscillatory single-electron transistor behavior. However, Q_0-insensitive memory architecture [42] has been proposed by Likharev to overcome this difficulty.

The purpose of this article is to discuss the issues which one inevitably encounters when one proposes a single-electron memory device as an integrated-circuit element. Single-electron devices are briefly reviewed in Section II. The room-temperature single-electron memory cell using natural nanostructure is discussed in Section III. Memory array organization is discussed in Section IV, and the reliability issues related with the small number of stored electrons are discussed in Section V. LSI is discussed in Section VI.

II. Single-Electron Devices: General Overview

A. Single-Electron Box

Because the physics of single-electron devices has previously been thoroughly reviewed in [1]–[3] and in the article in this Special Issue by Likharev [51], we focus on reviewing the key issues related to the engineering aspect required for the following argument. Fig. 1 shows the simplest single-electron circuit called a "single-electron box" [3], in which electrons can tunnel between a reservoir and a dot. This electron motion is controlled by the gate voltage. Moving an electron from the reservoir to the dot is not difficult by applying a voltage q/C, where q is the absolute value of one-electron charge and C is the capacitance of the dot to the gate electrode; however, the fluctuation in the charge on the capacitance which naturally arises from thermal energy is much larger than this. This charge fluctuation ΔQ and the corresponding fluctuation in the number of electrons Δn are expressed by the following equation:

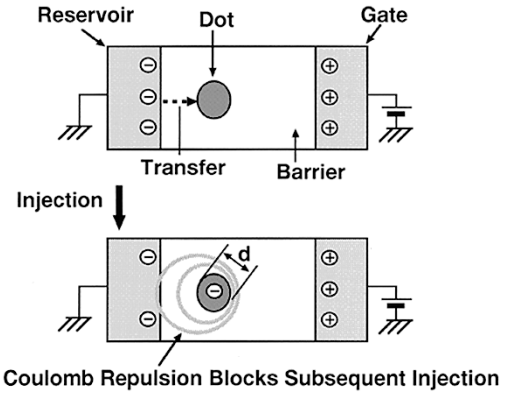


Fig. 1. The schematic view of the single-electron box.

$$\Delta Q = (2kTC)^{0.5} = q\Delta n \tag{1}$$

where T is the temperature and k is the Boltzmann constant. Assuming that C is 1 fF, which is a typical value for a submicron electrode, Δn is 18. In this regime, where Δn is much larger than one, the charge Q which is averaged during observation is considered to be an arbitrary value and is therefore treated as a continuous quantity. By contrast, when C gets very small approaching $q^2/(2kT)$, Δn approaches unity. In this regime, the charge Q remains an integer multiple of q. From the particle viewpoint, it is clear that the transferred electron blocks the transfer of other electrons due to the strong Coulomb repulsion in such a small structure (see Fig. 1). This is referred to as the Coulomb blockade effect.

The condition for the Coulomb blockade effect to appear, i.e., the Coulomb energy becomes comparable to the thermal energy, is plotted in Fig. 2. In earlier single-electron physics/device demonstrations [1], [2], submicron structures were used at cryogenic temperatures, i.e., at temperatures below 1 K. Room-temperature operations requires very small structures of less than 10 nm, much smaller than present lithography resolutions and difficult to achieve. There have been several tricks proposed to achieve this small size before nanolithography is established.

Fig. 2 is sometimes misleading, because some device operation principles require a stringent operating condition, which is "sufficiently below" the line in Fig. 2. The single-

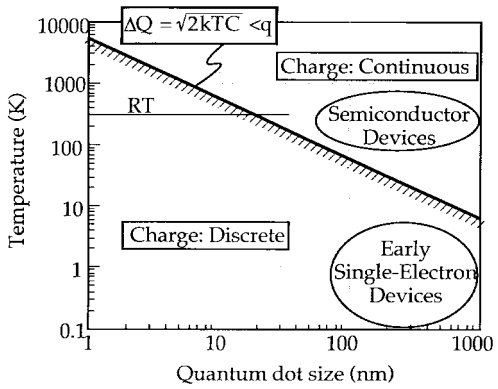


Fig. 2. Conditions for the Coulomb blockade. The self-capacitance of uniformly charged sphere is assumed in the calculation.

electron transistor is such an example. How far below the operating point the border line in Fig. 2 is, which corresponds to the ratio of the Coulomb energy to thermal energy, determines the half width of the current oscillation characteristics, which correspond to the gain of the logic and leakage current level (the characterization of the gain under finite Coulomb energy condition is described in [28]). This means the operating point should be well below the line. This means roughly less than 1-nm size is required for room-temperature operation [17]. On the other hand, floating-dot memory scheme using FET readout, which will be discussed below, relies on the Coulomb blockade for suppressing the stochastic variations of stored electrons, as will be detailed in Section V. Operating principle is continuously changed from the floating-gate-type classical memory to single-electron memory. Therefore, operation is possible at any point in the figure, even at above the border line at the expense of uniqueness and possible advantages of this principle.

B. Operating Principle

The operation of single-electron memory [10], [11] is compared with that of the single-electron box shown in Fig. 3. Something difficult to understand from the classical circuit viewpoint is that the potential of the dot V_t is not fixed to ground even if the dot is connected to the ground via the resistance. This is because arbitrary continuous charge transfer through the resistance is not always possible in such a regime, but only integer-multiples of an electron charge can be transferred through the resistance.

Because the resistance R has a linear current-voltage curve in a single-electron box, the charge Q_t is uniquely determined for a given gate voltage value V_g. In contrast, in single-electron memory the current-voltage curve is nonlinear, i.e., a finite threshold voltage is required to turn the resister into conductive. Because of this, combined with the quantized nature of charge, multiple Q_t values are stable for a given gate voltage and single-electron memory operation is possible. A well-known means of forming nonlinear resistance is to use multiple tunnel junctions [9]–[11]. However, nonlinear resistance does not necessarily have to come from multiple tunnel junctions. Other general nonlinear resistances, such as various built-in potentials in semiconductors, can be used. The larger degree of freedom for forming nonlinear resistance is one advantage of using semiconductors for single-electron memory.

Memory operation is achieved as follows. As the gate voltages increases, the voltage V_t, which is applied to the nonlinear resistance, also increases. When V_t reaches V_{b1}, the threshold voltage, the nonlinear resistance R becomes conductive and an electron is transferred from the reservoir to the dot. Just after this transfer, V_t decreases by q/C_{tt}, and R again goes into a high resistance state (C_{tt} is the total capacitance of the storage node). This blocks the transfer of another electron. If the gate voltage is further increased, the number of electrons in the dot increases with every q/C_{gt} gate voltage increase. The case of decreasing gate voltage is similar. The resulting hysteresis can be used for memory. The number of stored electrons are precisely controlled by the Coulomb blockade effect. The precision is determined by the strength of the Coulomb energy relative to the thermal energy.

C. Sensing Schemes

Storing precise number of electrons is not enough to obtain a memory cell. Sensing the stored charge is another essential operation.

The basic principle to sense a small number of electrons is to reduce the capacitance coupled to the storage node. This is because the voltage signal is given by the charge divided by the capacitance. Based on this principle, DRAM-type charge sensing is not suitable because the large bit-line capacitance is involved in the signal development.

Placing a local amplifier to the storage element is a better scheme. This scheme was used in the single-electron circuits operated at low temperatures by Fulton *et al.* [9] and Nakazato *et al.* [11]. However, the local wiring between storage node and the input port of the amplifier is inevitable and considerably reduces the signal.

A further improved scheme embeds the storage dot into the amplifier, and we call this a one-transistor floating-dot memory. This allows us to have a large voltage signal by reducing parasitic capacitances. If we can achieve the total coupled capacitance (the precise formula will appear below) of 0.2 aF, a 1-V threshold-voltage shift appears.

The operation of the floating-dot scheme is elucidated by the energy diagram shown in Fig. 4(a). Because a barrier region is formed between the reservoir (this is the channel or the source) and the dot, the current-voltage curve between these nodes is nonlinear with offset voltages. By applying a positive gate voltage, an electron is transferred to the dot at the critical gate voltage value. At this moment, the potential in the dot region is decreased and this blocks the transfer of other electrons. This is the Coulomb blockade effect. As shown in Fig. 4(b), the trapping of an electron in the dot shifts the threshold voltage of the FET. Therefore, by sensing the current difference between the two states, the stored information can be read.

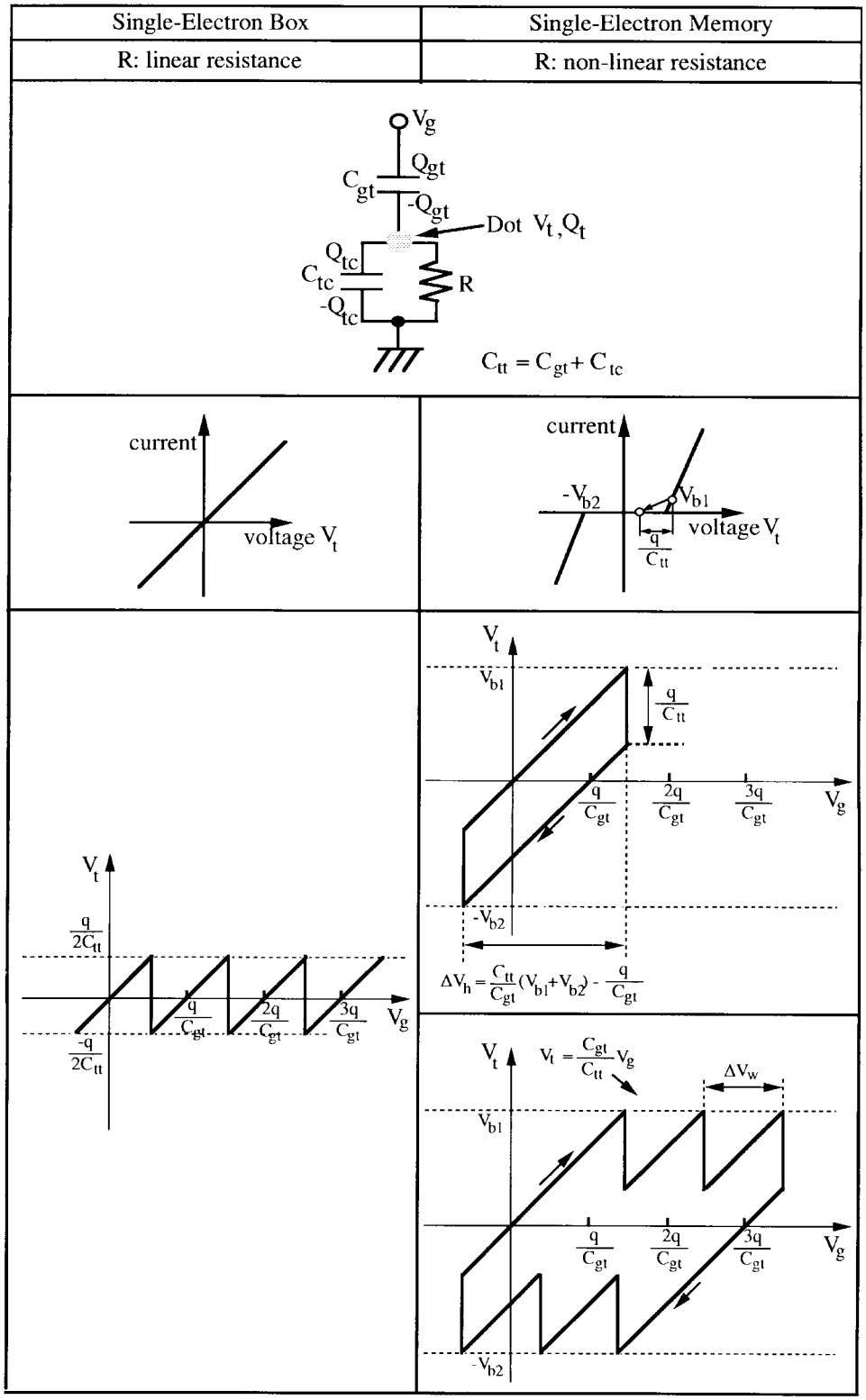


Fig. 3. Comparison between the single-electron box and single-electron memory. Nonlinear resistance characterized by the threshold voltages V_{b1} and V_{b2} is essential for the memory operation: (a) circuit; (b) IV curve of resistance R; (c) storage node potential.

D. Operating Conditions

Let us quantitatively analyze the memory operation. The equivalent circuit of the device is shown in Fig. 5(a). The electrostatic energy of this circuit U is given by

$$U = Q_{gt}^2/(2C_{gt}) + Q_{ts}^2/(2C_{ts}) + Q_{tc}^2/(2C_{tc}) + Q_{fc}^2/(2C_{fc}) - (Q_{gt} + Q_{fc})V_g \quad (2)$$

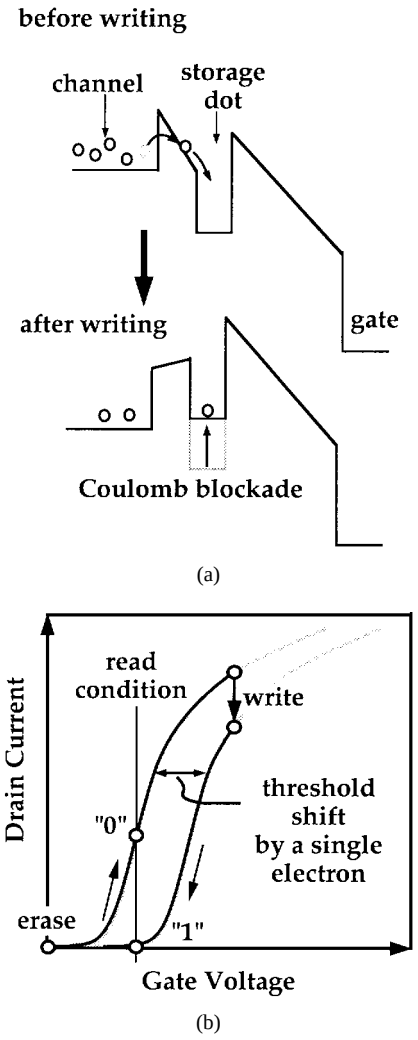


Fig. 4. (a) Schematic energy diagram for the proposed single-electron memory. (b) The schematic current voltage curve of the memory device.

where C_{gt}, C_{ts}, C_{tc}, and C_{fc} are defined in Fig. 5(a), and Q_{gt}, Q_{ts}, Q_{tc}, and Q_{fc} are charges related to the capacitances having the same subscript. By eliminating dependent variables, the equation is simplified

$$U = \left[(qn_t)^2 + 2qn_tC_{gt}V_g - C_{fc}C_{tt}Vg^2 - C_{gt}(C_{ts} + C_{tc})V_g^2\right]/(2C_{tt}) \quad (3)$$

where n_t is the number of trapped electrons in the storage node and $C_{tt}(= C_{ts} + C_{ts} + C_{tc})$ is the total capacitance related to the storage node. According to the global rule [1]–[3], the dynamics of n_t are semiclassically determined so that U is minimized at a given gate voltage. The fluctuation at finite temperatures is also characterized by this energy function (quantified discussion should be related with the concerning time scale as it always is in noise characterization). The charge in the channel Q_c is given by

$$Q_c = -Q_{fc} - Q_{tc} = -C_{fc}V_g - C_{tc}V_t \quad (4)$$

$$= -C_{fc}V_g - C_{tc}[(C_{gt}/C_{tt})V_g - qn_t/C_{tt}] \quad (5)$$

$$Q_c = -C_{fc}V_g - (C_{tc}/C_{tt})(C_{gt}V_g - qn_t). \quad (6)$$

Here, we presumed that the channel charge in the FET is a continuous quantity above threshold voltage, although the analysis can also be applied to the case of the single-electron transistor in place of the FET. The threshold voltage $V_{\rm th}$ is the gate voltage which corresponds to a specific channel charge. By increasing n_t by one, the threshold voltage is shifted by

$$\Delta V_{\rm th} = (C_{tc}/C_{tt})(q/C_{gc}) \quad (7)$$

where C_{gc} is the capacitance between the gate and the channel and is given by $C_{fc} + (C_{tc}/C_{tt})C_{gt}$. The readout voltage can be increased by reducing C_{gc}.

The conditions required for memory operation are as follows. First, the channel region of the device should be as small as the storage dot. Next, the current reduction ratio between "1" and "0" should be larger than critical value, which is here tentatively set to be e (base of the natural logarithm) for making the formula simple. The current reduction ratio of e is achieved if the threshold shift $\Delta V_{\rm th}$ is larger than kT/q, since drain current is proportional to $\exp[-qV_{gs}/(nkT)]$, where n is assumed to be ideally unity. Therefore, the following condition is required:

$$(C_{tc}/C_{tt})(q/C_{gc}) > kT/q \quad \text{(Readout Condition).} \quad (8)$$

The multiple-state stability of the circuit is achieved only if the hysteresis width is positive. This is satisfied when [14]

$$q/C_{tt} < V_{b1} + V_{b2} \quad \text{(Multiple-State Stability Condition).} \quad (9)$$

Here, V_{b1} and V_{b2} are the threshold voltages of the forward and backward current flow through nonlinear resistance R in Fig. 5, respectively. Another requirement for the stability of the stored states is that the leakage current of the nonlinear resistance below the threshold voltage of the resistance should be low enough. This determines the retention time. The leakage current may originate from the direct tunneling from the reservoir to the storage dot or tunneling via an undesired midgap state in the barrier region.

The Coulomb blockade effect, by which the transfer of the second electron is precluded, is effective if

$$q^2/(2C_{tt}) > kT \quad \text{(Coulomb Blockade Condition).} \quad (10)$$

As $q^2/(2C_{tt})$ gets larger than kT, the probability that the number of stored electrons will deviate from the target value gets higher. This means that memory control is degraded. To satisfy all of the above conditions at room temperature, C_{gc} and C_{tt} should be smaller than 3 aF.

III. Room-Temperature Operation Device

A. Nanocrystalline Silicon

To investigate the above scheme at room temperature, we examined various possibilities. However, if we define the channel and dot using lithography, the operating temperature was estimated to be far below room temperature.

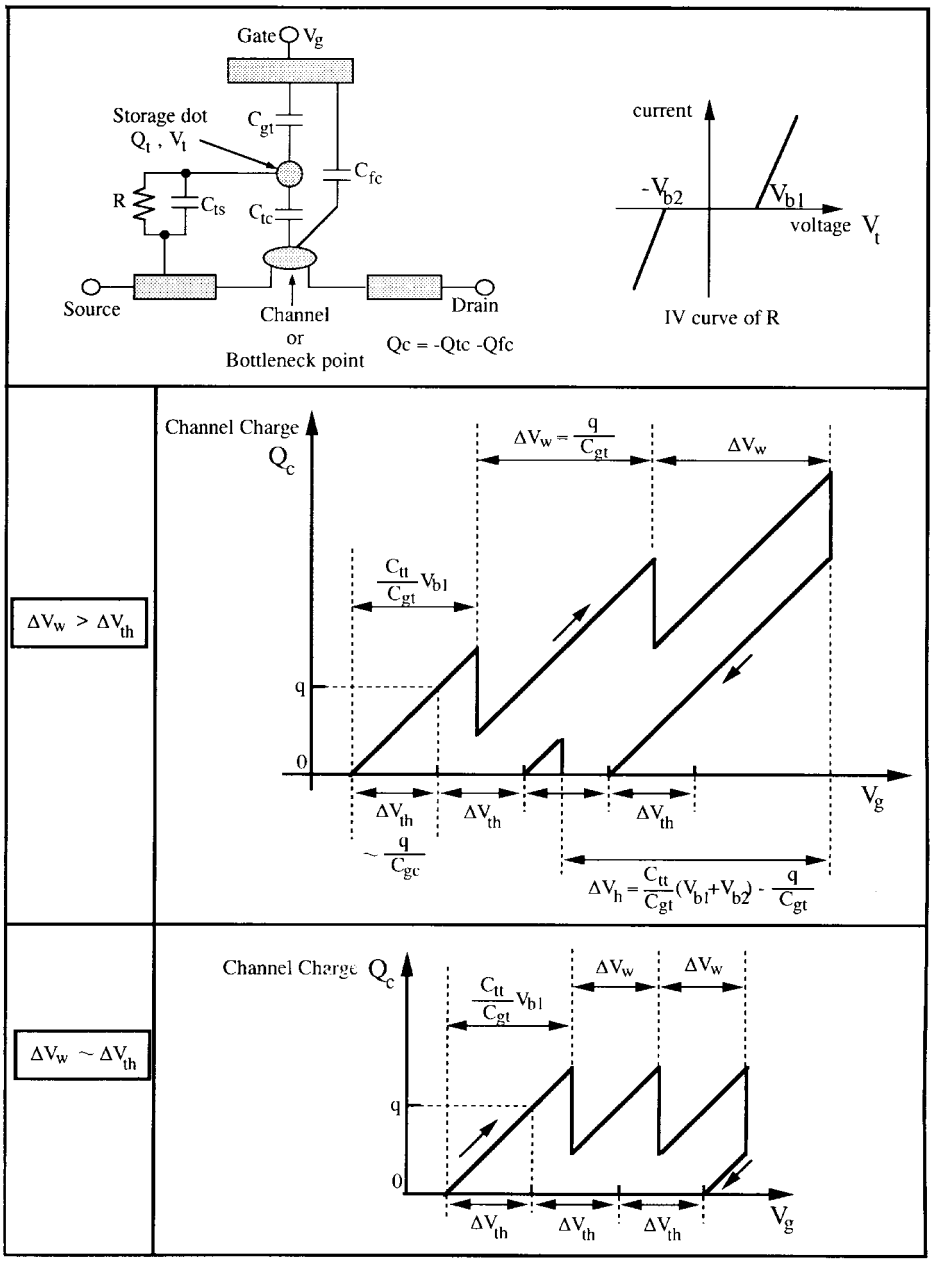


Fig. 5. The equivalent circuit and typical behavior of the proposed single-electron memory. Two types of behaviors are possible depending on the single-electron write period ΔV_w and threshold voltage shift $\Delta V_{\rm th}$. ΔV_h is the width of the hysteresis: (a) equivalent circuit and (b) channel charge versus gate voltage.

Our solution was to use natural nanostructures. When we started this work, two of the authors had been working on depositing thin polycrystalline silicon film, which was to be used for thin-film transistors in large scale SRAM cells, replacing older highly resistive poly-Si load. The film thickness seemed to be extended down to 10 nm or below. The poly-Si was suitable for reducing parasitic capacitances around the active region when it is surrounded by silicon dioxide film. We decided to use this technology to achieve an ultralow capacitance device.

The fabricated device was an ultrathin-film transistor with channel poly-Si width and gate lengths of 100 nm. The channel poly-Si (or nano-Si) was as thin as 3.4 nm on the average (Fig. 6). This nano-Si was deposited as amorphous Si and crystallized at 750°C by annealing. The cross-sectional TEM photograph of the film (Fig. 6) shows clear lattice images, which means that it consists of crystalline Si grains. The film thickness varies from one position to another, ranging from 1–5 nm, which is very important for electron transport, as discussed later. The gate oxide was 150-nm thick, which was intended to reduce capacitance between the gate and the channel, however, it turned out to be thicker than it is needed later. The electrical property of the nano-Si was found to be very different from those of the thicker poly-Si.

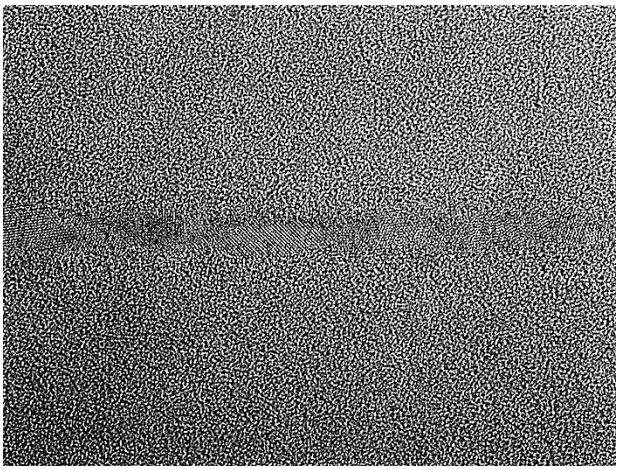


Fig. 6. Cross-sectional TEM photograph of the channel poly-Si.

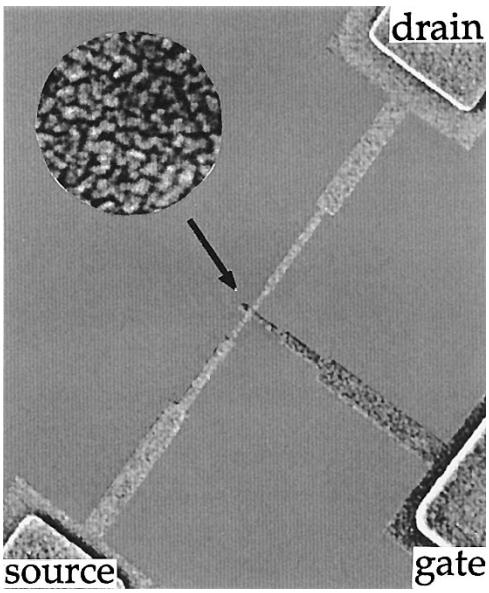


Fig. 7. The SEM microphotograph of the fabricated memory. Nano-Si is sandwiched by amorphous silicon dioxide.

B. Nanocrystalline-Silicon Memory Characteristics

The fabricated device (Figs. 7 and 8) worked as a single-electron memory at room temperature, just as in the model discussed in Section II. We measured the drain current as we swept the gate voltage up and down between 10 V and $V_{g\max}(>10$ V), the maximum gate voltage, as shown in Fig. 9. When $V_{g\max}$ is less than 40 V the current is almost independent of the sweeping direction. However, all of a sudden, when the maximum gate voltage is 44 V, clear hysteresis is observed. The threshold shifts by about 10 V. We also observed the second threshold jump at about 56 V. Again, the threshold shifts by about 10 V. It should be noted that no hysteresis has been observed in poly-Si thin-film transistors fabricated in the same process line with a thicker channel poly-Si (10–100 nm). Therefore, it is clear that the hysteresis is caused by the thinness of the fabricated channel. The memory effect is very stable, lasting more than 1 h.

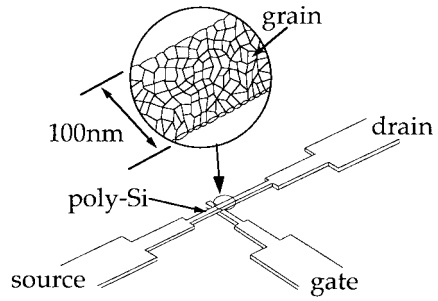


Fig. 8. Fabricated nano-Si memory structure and enlarged active region.

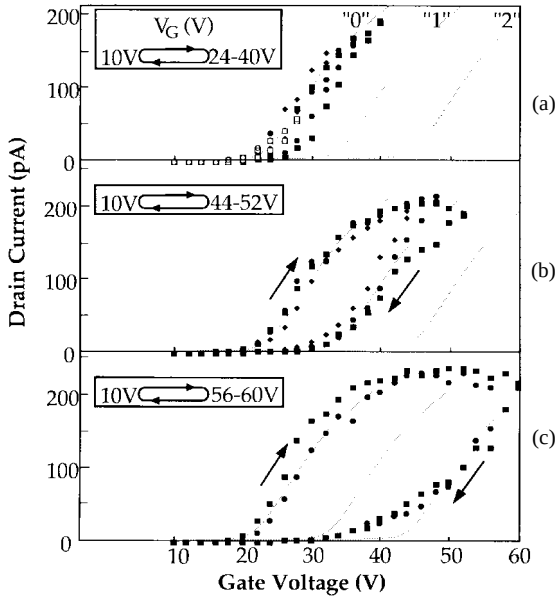


Fig. 9. Measured drain current versus gate voltage. The drain-source voltage is 50 mV. The gate-voltage sweep rate is 4 V/min. The maximum gate voltage in a sweep loop is: (a) 24 V(○), 28 V(□), 32 V(◆), 36 V(●), 40 V(■); (b) 44 V(◆), 48 V(●), 52 V(■); and (c) 56 V(●), and 60 V(■).

One plausible model which explains the observations, particularly that the hysteresis is observed only when the silicon thickness is below 5 nm, is based on the random thickness variations in the film. In such a sub-5-nm film, a very strong vertical quantum confinement effect is expected. We analyzed the statistical properties of the film thickness from the TEM photograph and obtained an average thickness of 3.4 nm, standard deviation of the thickness of 0.95 nm, and autocorrelation length, obtained from of 2.9 nm. Based on this data, a potential landscape was created by using the Monte Carlo method. A highly random potential, which may be called "the nanometer Grand Canyon," is formed due to the thickness variations.

If we apply a positive voltage to the gate, the film becomes conductive when a percolation channel is formed from source to drain. This corresponds to the threshold voltage of the device. Note that the current path is much narrower than the actual poly-Si width, less than 10 nm. The onset of conduction is governed by a very small bottleneck region (roughly 10 nm in diameter) in the percolation

path [15]. This bottleneck corresponds to the "channel" in Fig. 5(a), and the rest of the current path is regarded as the source and drain. Low-energy pockets isolated from the percolation path are also formed. These correspond to the floating dot shown in the model in Fig. 5(a). If we increase the gate voltage above the threshold voltage, the potential of the current path is fixed to the source, because it is conductive. However, the potentials of the other nonconductive regions are increased, which creates a local electric field between the current path and the isolated dot (or dots). Finally, one electron is transferred from the current path to one of the isolated dots and trapped. This trapping causes a quantum jump of the threshold voltage, and it can be detected as a discrete current change.

If the threshold jumps are caused by single-electron trapping in a storage dot, characteristic quantities related to threshold shift, $\Delta V_{\rm th}$ and ΔV_w defined in Fig. 5(b), should be related to the capacitances, which is shown in inset equations in Fig. 5. To confirm this, we performed three-dimensional capacitance simulations based on a realistic device geometry. We assumed that both the storage dot and the lateral size of the bottleneck were 10-nm across. The simulated C_{gt} is 2.0 $\times$ 10^{-20} F, and C_{gc} is 2.0 $\times$ 10^{-20} F. The C_{tc} depends on the distance between the storage dot and the bottleneck, however, it is about 1–2 $\times$ 10^{-18} F. The total capacitance of the storage node is 2 $\times$ 10^{-18} F. Putting these values into the equations, we obtain $\Delta V_{\rm th}$ and ΔV_w of 8 V, which is close to the values obtained in experimental observations.

Although the device characteristics are far from what can be used in real applications, the possibility of room-temperature operation device with natural nanostructures became real through this experiment.

IV. Array Construction

Although memory operation at room temperature was demonstrated, the device had to be improved in many characteristics (speed, voltage, size). Moreover, even if all these are solved, memory integration requires more than just a good hysteresis device. One has to organize a cell array, in which an xy matrix of memory cells share various components. This is necessary because, without it, one needs one billion sense amplifiers (and many other components to control the source, drain, and gate) to organize the 1-Gbit memory, which is far larger than the array counterpart.

A. Array Architecture

There is a long history regarding how one organizes the memory array. Basic organization is the use of a word line, which controls the horizontal (x-direction) "row" of cells, and a data line, which controls and provides input/output signals to the vertical (y-direction) "column" cells. The basic idea is to access the cell placed at the cross point of the selected row and column. But the control voltages are applied to cells other than the selected cell in various forms, and therefore it is more accurate to say that the entire

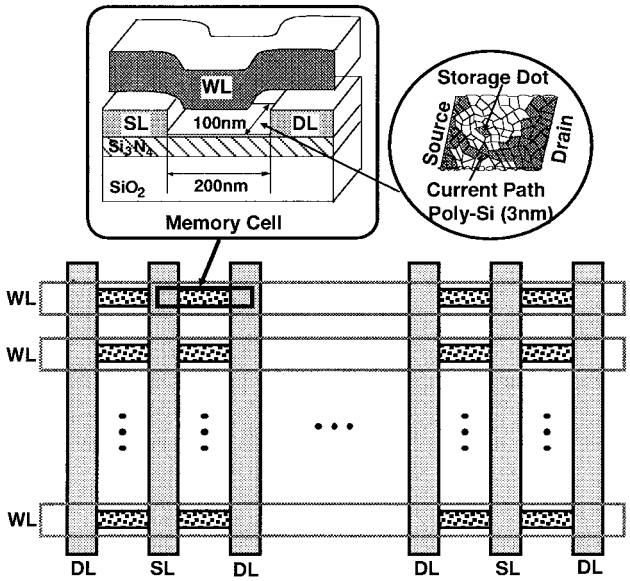


Fig. 10. Schematic structure of ladder-shaped Coulomb memory cell array. Word line (WL), data line (DL), and source line (SL) are poly-Si.

xy-matrix collectively operates. Many array and control architectures have been devised for DRAM's and flash memories.

Maybe because of the physics-oriented early research history of single-electron devices, there was no research interest on array-level operation until our report in [15], in which an 8 $\times$ 8-array organization was investigated and experimentally demonstrated. This experiment uses the nano-Si-based single-electron memory, which presumably contributed to make this early move into integrated-circuit-level research possible.

Because the logic function of one-transistor memory cell structure is similar to those of flash memory cells, learning from their array organization might be a good starting point. Our array organization is influenced by those flash-memory organizations.

The basic device structure is essentially the same as the one described in Section III, however, it is significantly improved in the following aspects. The gate, or the word line, is parallel to the channel and covers all the channel region between source and drain (Fig. 10). This arrangement is essential for compact cell layout. Because of the full coverage of the channel, the parasitic source and drain resistances are much lower for this device. The ultrathin poly-Si in this device is 3 nm, thinner than 3.4 nm for the earlier device in Section III. The gate oxide thickness is reduced from 150 to 30 nm to lower the operating voltage. The previous devices required 90–100 V gate voltage, while this device works at 15 V, which is comparable to voltages used in flash memories.

Memory-cell array consists of ladder-shaped poly-Si lines, in which channel poly-Si corresponds to a rung and data/source poly-Si lines correspond to side pieces (Fig. 10.) A group of channel poly-Si's covered by a word line constitutes a sector, the basic write/read unit. The

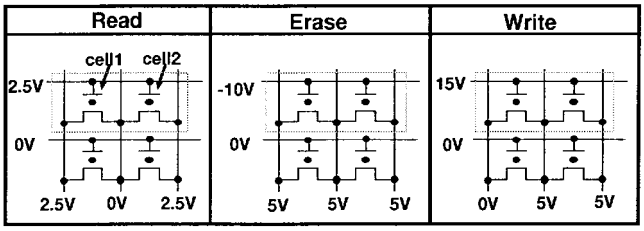


Fig. 11. Memory-cell array operating voltages. Four cells are shown as an example. Target cells are cell1 and cell2, and the other two cells are not target cells but are inevitably biased in this array organization.

source line is shared by two adjacent cells to reduce the cell area, yielding a $6F^2$ cell area, where F is the feature size.

One feature of this architecture is the addition of erase operation to write and read operations. The purpose of this erase is to avoid successive write operation on the same cell. This is needed because single-electron memory has multiple stable states, as shown in Section II, and therefore, if a cell is written successively multiple times, the final cell state cannot be controlled. By introducing erase before every write, this unpredictability is overcome.

Another feature is that all the operation of this device is word-line based. All cells coupled to a word line is simultaneously erased/written/read (Fig. 11). The cell itself has current gain (as does a flash memory cell). By storing a small number of electrons, cell current is almost cut off. This current change is easily sensed by conventional sense amplifiers, although the test chip does not include a sense amplifier.

The most challenging aspect may be write, in which a "1" is selectively written to a cell with high word-line voltage, while in another cell coupled to the same word line, "0" has to be retained. Our scheme is to apply positive bias to the data line of the cells for "0" and 0-bias to the cells for "1" as shown in Fig. 11 to make this selection possible.

Another new architecture is the verify operation. Verify, which has been well known in flash memory designers [44], compensates the characteristics scattering by using peripheral circuits. To be concrete, each time write is performed, the finishing of the write is checked by reading out the cell. If the write is not completed, the write is repeated and checked until the cell state reaches the predefined written state. Memory cells inevitably have cell-to-cell scatterings, which include process-induced inter-cell variations, background-charge-induced variation, and stochastic variation of electron count. Our nano-Si-based memory utilizes the natural structure, and the scattering should be larger than those of more controlled devices. Verify suppresses all those variations with the help of peripheral circuit techniques.

B. Measurement

The fabricated 64-bit memory array is shown in Fig. 12. The memory-cell area is as small as 0.415 μm^2. Most of the feature size is 0.25 μm, except the channel uses 0.1 μm width.

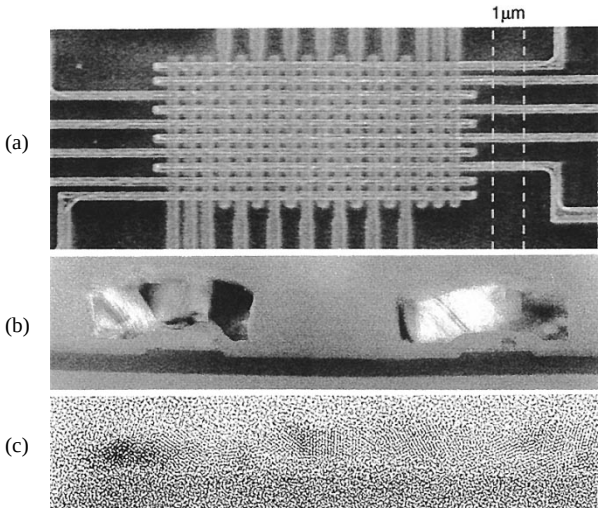


Fig. 12. Microphotograph of an 8 × 8-bit memory-call array: (a) SEM view showing horizontal word lines and vertical data/source lines; (b) cross-sectional TEM view across word line and channel; and (c) enlarged TEM view of nano-Si. Word-line pitch is 0.55 μm.

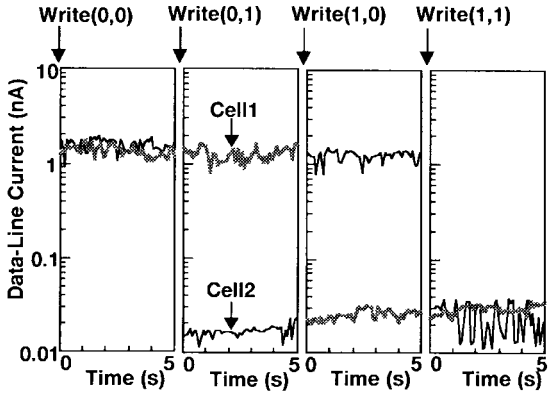


Fig. 13. Repeated erase/write/read of two memory cells sharing word line and source line. Word/data-line voltages are those in Fig. 11, except read is at 0.1 V/1 V, respectively. The write/erase is completed within 1 ms.

Selective write/read of the memory array is one of the difficult hurdles for a new memory device. Our scheme works well in our experimental array (Fig. 13). The data line current after write is two-orders of magnitude lower than that after erase.

The fact that the device is working as a single-electron-based principle is shown in Fig. 14, where the write voltage is reduced to 9 V to make real-time current measurement possible. Each abrupt current drop corresponds to storing one electron. Important observation in Fig 14 is the electron injection time constant gets exponentially longer every time an electron in injected. This is a direct observation of Coulomb blockade.

An advantage of single-electron memories is faster write and erase than those of flash memories. This is because the number of electrons stored or erased is dramatically lower in the single-electron memory, about five in this device, as

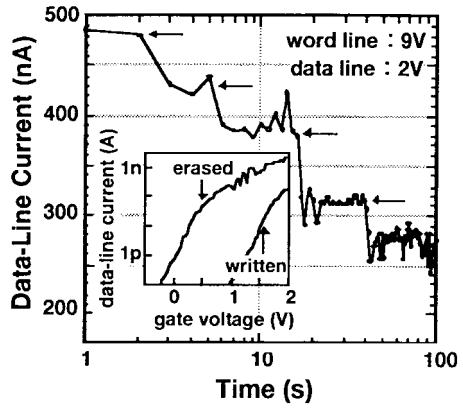


Fig. 14. Data-line current during write at 9 V showing one-by-one trapping events. The trapping time constant gets exponentially longer each time an electron is trapped, which directly shows Coulomb blockade illustrated in Fig. 1.

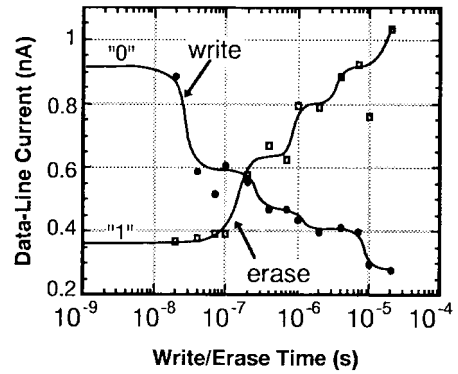


Fig. 15. Write/erase characteristics. The word/data line voltage for current measurement is 1 V/1 V, respectively.

is contrasted to about 10^5 in a flash memory. Write/erase is typically completed in 10 μs (Fig. 15), corresponding to 50-Mbytes/s bandwidth, two-orders faster than for typical flash memories, if the number of bits connected to a word line is extended to 512 bytes (typical sector size of flash memories).

Another feature of single-electron memories is high endurance against repeated write/erase cycles. Although the number of measured devices is limited thus far, because measurements require long times, 10^7-cycle operation is confirmed (Fig. 16).

The retention time of the devices is short for a nonvolatile memory, typically 1 h to a month. Refreshing is required for this present device. This might be improved by further thinning of the poly-Si film. More comparison with conventional memories including future prospects is discussed in Section VI.

C. Device-to-Device Variations

Device-to-device scattering has been the major concern against serious consideration of single-electron device in mainstream electronics [1]. As for the nano-Si-based memory, the scattering should be severer because of the inherent randomness in the structure.

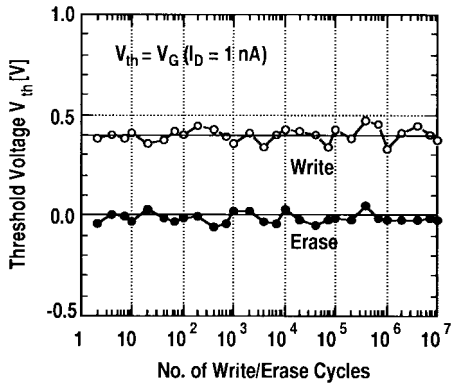


Fig. 16. Endurance characteristics versus write/erase cycles.

The effect of the verify is clearly shown in Fig. 17. Although the control of the threshold voltage is not perfect after verify, it is surprisingly good if one recalls that these devices are fabricated in our test laboratory, not a manufacturing line.

However, the verify has its limit. In array structure, the same word line voltage has to be applied to all the cells under the word line. Under this constraint, we had to increase the write time up to 1 s to obtain the tight distribution in Fig. 17. Tighter control of the device threshold voltage is required.

V. Error Rate and Low-Charge Limit

Although the array experiments have shown positive aspects of the single-electron memory, there should still be a basic concern as to whether a reliable operation needed for gigascale integration is possible with such a small number of stored electrons. In conventional memory devices, which represent 1 bit with more than 10 000 electrons, the stochastic electron-count scattering, which is proportional to $\sqrt{N}$, is negligible because the total electron count N is relatively much larger than the scattering. However, when N is small, $\sqrt{N}$ becomes relatively large. This becomes severer if we consider that even a single cell should not go beyond the worst-case design point in LSI design, however, the probability of such a fail event might not be negligible under LSI conditions.

In this section, using the single-electron memory device described in Section IV, the error rate of the single-electron memories is examined and related to the low charge limit of the semiconductor memory device.

A. Electron-Counting Measurement

By using the memory device similar to the one used in array ($W/L = 0.1/0.2$ μm), each instance of electron injection is observed at room temperature as an abrupt drain-current reduction (Fig. 18). To make real-time observation using HP4156A with time resolution of 0.1 s possible, we set the gate voltage to 12 V. Sometimes the second electron injection was observed (Fig. 18, 65th run). By repeating the same measurement 100 times, we have obtained the stochastic characteristics of stored electrons.

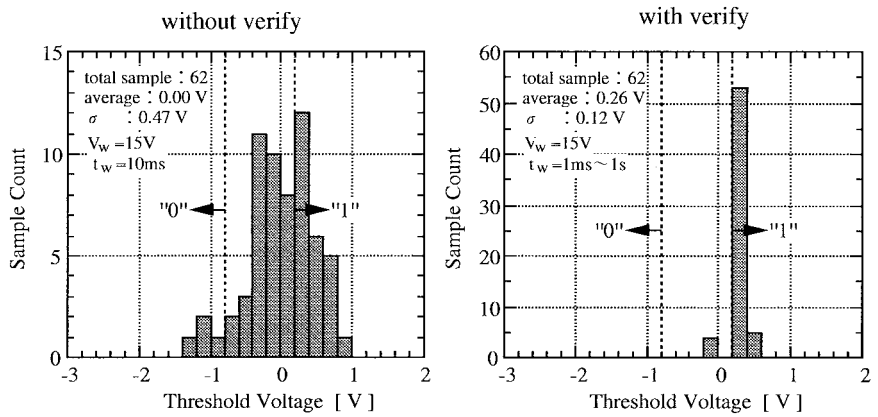


Fig. 17. Threshold voltage distribution after write in an array.

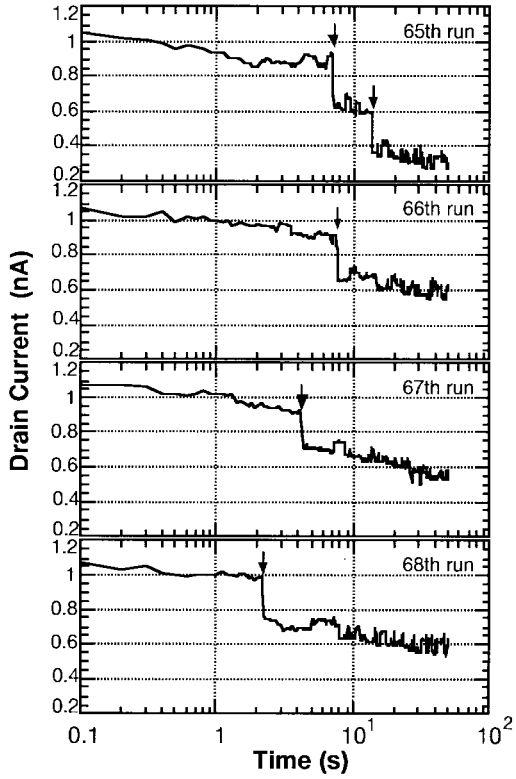


Fig. 18. Real-time electron counting measurement at write voltage of 12 V. The electron injection into a storage dot is indicated by an arrow. Four successive runs are depicted from 100 runs. An abrupt current reduction corresponds to 0.6-V threshold shift. The drain voltage was 10 mV.

The average injection time (t_1) of the first electron is 12.9 s (Fig. 19). The time evolution of the probabilities (Fig. 20) shows clear Coulomb blockade effect, i.e., the probability of the second electron injection is much lower than the value expected for Poisson process. For example, probability of two-electron storage is expected to be half of those of zero-electron and one-electron storage at t_1 according to the Poisson process; however, the former is only 1/6 of the latter in the experiment.

The single-electron-level control of charge is elucidated in the standard deviation σ of charge (Fig. 21). The σ is 0.6q and weakly depends on time after 10 s. By contrast, σ

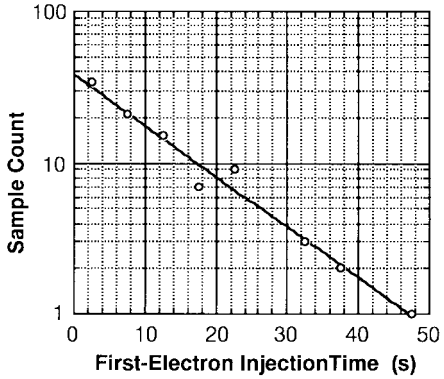


Fig. 19. The histogram of the first-electron injection time. The results fit well with the exponential decay expected for single-time constant process. The time constant is 12.9 s.

is proportional to time t according to the Poisson process, $\sigma = t/t_1$.

B. Dynamic Coulomb Blockade Model

All these measured results provide a unique database to check the validity of Coulomb blockade model in the dynamic regime. Here, the dynamic regime corresponds to transient conditions before energy minimum is reached.

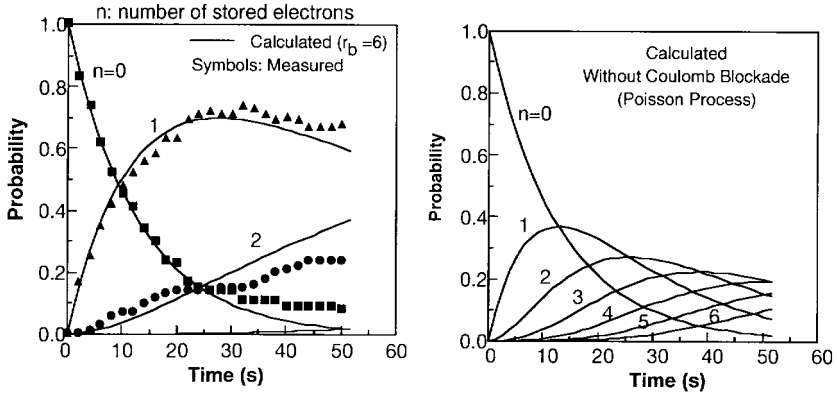
The measured data agree excellently with our dynamic Coulomb blockade model (Figs. 20 and 21). The basic idea of our model is that the Poisson process is modified under Coulomb blockade influences so that the injection time gets longer by a factor of r_b (blockade factor) as the stored electron count is incremented. Assuming $n-1$ electrons are already stored, injection time of the nth electron is given

$$t_n = r_b^n t_1.$$

r_b represents the potential change due to one-electron injection and is approximately given by

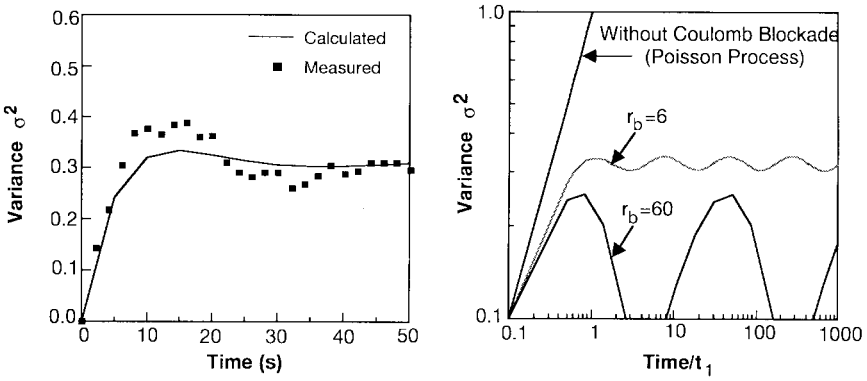
$$r_b \sim \exp\left[q^2/(2kTC_{tt})\right].$$

Here, C_{tt} is the total capacitance of the storage dot. The probability of n-electron stored state $P_n(t)$ is governed by



(a) (b)

Fig. 20. The time dependence of probability distribution of stored electrons: (a) shows the experimental results combined by the Coulomb blockade model calculation result and (b) shows different behavior when we neglect Coulomb blockade (this corresponds to Poisson process.)



(a) (b)

Fig. 21. Comparison of electron-count variance between experiment and calculation: (a) shows good agreement between the measured result and the simulation result; it also shows sub-one-electron control of electron count in this device and (b) shows grand behavior of the simulation result and the dependence on Coulomb blockade factor r_b.

a simple Markov process and is expressed as

$$P_n(t,t_1) = \int_0^t P_{n-1}(t-s, r_b t_1)\exp(-s/t_1)/t_1\, ds$$
$$P_0(t,t_1) = \exp(-t/t_1).$$

$P_n(t)$ has been analytically obtained by successive integration of this equation. The only parameters in this model are t_1 and r_b. t_1 is experimentally determined as described above, and r_b is determined to fit the results. However, the capacitance C_{tt} (1.7 aF) for this r_b value is consistent with the 10-nm dot in the nano-Si. The overall behavior of the model is shown in Fig. 22. A new finding in this calculation is that the variance σ^2 shows periodic oscillation versus logarithm of time. A peak corresponds to the transition from n to $n+1$ electron state and a valley corresponds to the stable state, in which electron count is fixed. Therefore, this oscillation can be called "uncertainty beat" due to charge quantization. This is observed in the experiment (Fig. 21, only the first peak), although it is not sharp due to the low r_b value.

C. Low-Charge Limit of Memory Device

Based on the above results, we can answer the following fundamental questions: what minimum charge must be used for a memory device and does Coulomb blockade have an impact on this limit? Although there are many failure modes which might eventually limit memory operation, here we focus our discussion on the intrinsic statistical charge variations, which are caused by the Poisson nature of electron injection. This includes a failure of reading wrong data because the stored charge happens to be less than the typical charge amount.

The important finding in the above experiment and calculations is that the tail of the number distribution is very sharp, much sharper than the Gaussian distribution. Even without verify, the number of stored electrons is controlled to average ± 2 electrons without error. Here we need a criterion to define what "without error" means. We used a criterion of less than 1000-fit error-rate when 1-Gbit memory chips are made. Here, fit is the unit representing the failure rate, defined by the rate of one failure per an hour when 10^9 chips are operated. With verify, the stored electrons are controlled to average ± 1 electrons. If we assume that 20% electron-count deviation is tolerable, total ten-electron storage is feasible without verify and five-electron storage is feasible with verify. These are the minimum electron count to achieve this reliable operation when we use the 10-nm dot size.

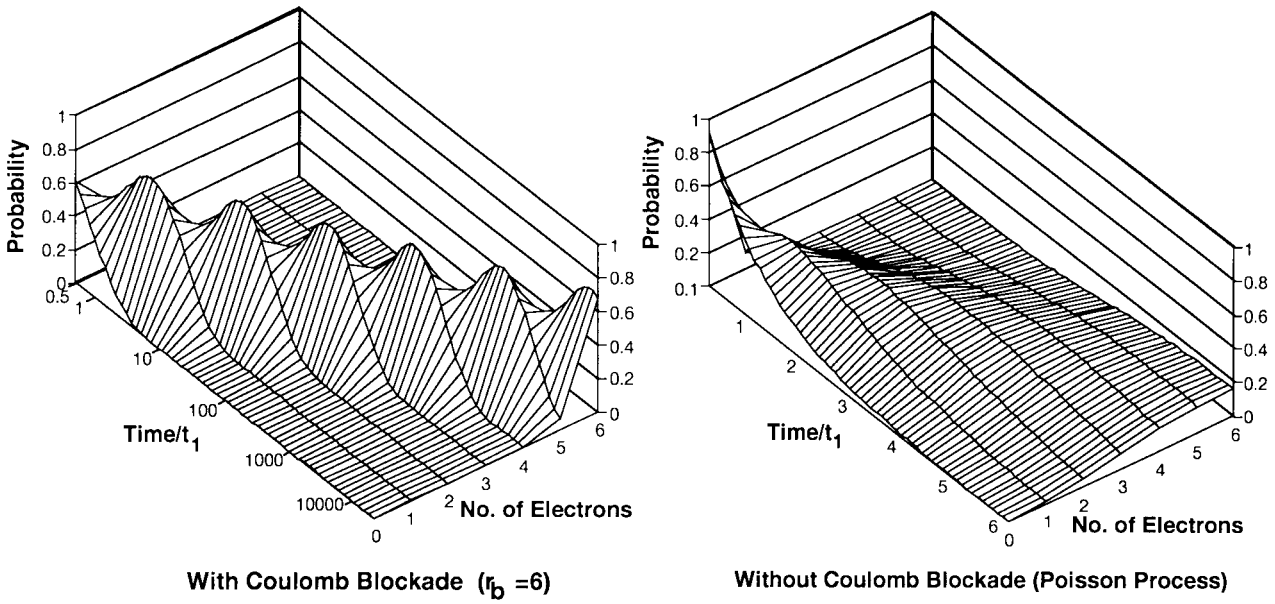


Fig. 22. Simulated time evolution of probability distribution function, which demonstrates the self-stabilizing nature of the distribution under the Coulomb blockade condition.

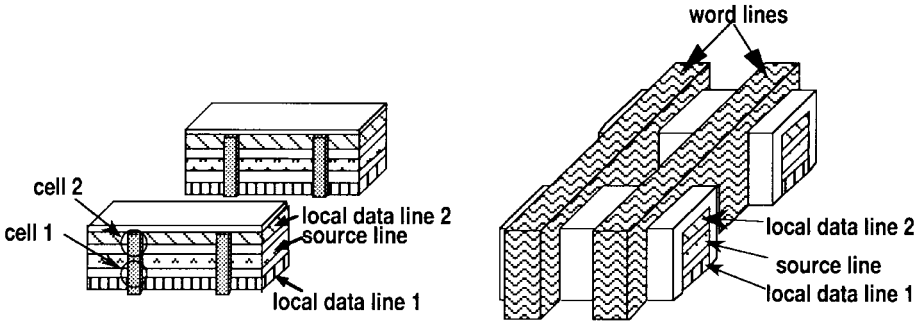


Fig. 23. Vertically united cell structure, which integrates two cells in a contact area. The nano-Si is deposited on the sidewall of the data line and source line stack.

VI. LSI

Single-electron memory, which succeeded room-temperature operation in 1993, has grown steadily to 64-bit integration in 1996 [1] as described in Section IV. However, the gap between 64-bit and the target, gigascale integration, is large. Also, the chip-level advantage over conventional memories has yet to be clarified. To fill this gap, we started a project in which we make a prototype of LSI circuits to gain insights into the chip-level potential of the single-electron memory and also to develop key circuit/device technologies required for integration.

A. Positioning Among Memory Architectures

We have defined the positioning of this emerging technology to the smallest cell-area technology, which provides minimum bit cost. Although the single-electron memory, which inherently has better scalability over conventional memories, might eventually replace DRAM's and flash memories in the long time frame (this might be 16 Gbit or later), there is difficulty if we try to benefit from this device in a shorter time frame. The cell area is determined by the word and data line pitches and is difficult to lessen without lithography advances.

The proposed vertically united cells (VUC) structure [43] (Fig. 23) is to go beyond this limit by integrating upper and lower cells in 4 F^2 contact-cell area, where 2 F is the word and data line pitches. The nano-Si-based memory cell as described above has a much simpler structure than conventional memory cells. Basically, it does not need capacitance for a DRAM cell nor a bulk MOSFET. Here we utilized this degree of freedom to make the memory current direction vertical to the substrate and unify 2-bit cells in a contact area. Note that two cells share many components, such as word line, source line, channel silicon, and all of these components are simultaneously fabricated in both cells. Therefore, the increase of process steps to go from a one-storied cell to two-storied cells is only 5%.

Stacking more than two cells by this VUC structure seems to arouse difficulty. One is that it requires deep etching of word lines on very high aspect ratio, and the other is that taking contact to each of the stacked data lines becomes more difficult and area consuming.

B. CMOS/Single-Electron-Memory Hybrid Integration

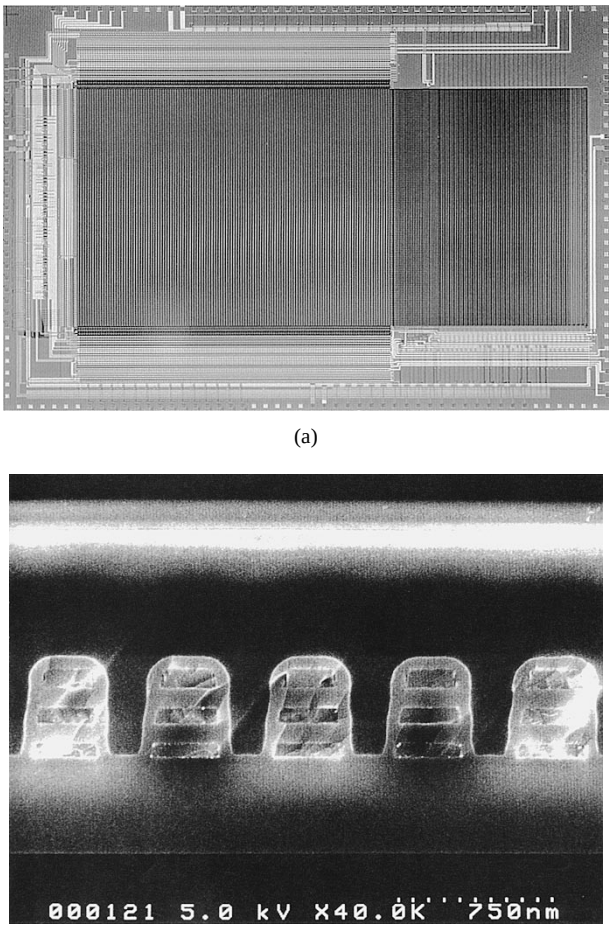
Combining CMOS peripheral circuits with the single-electron memory device extends the horizon of this new technology.

The major obstacle against LSI is cell characteristics variations, which include process/temperature/voltage variations and stochastic electron count variations inherent in single-electron memories [4]. Stable read/write is accomplished using dummy-cell-referenced verified read/write architecture. A dummy cell, which has the same structure as the memory cell, is used. Because the same dummy cell is referenced for both verified write and read, the memory cell threshold is automatically controlled around the dummy-cell threshold. This dramatically improves the variation margins.

Conventional folded-data-line scheme used in DRAM's [46], however, generally has considerable area penalty, because the same word line cannot be shared by its spouse data line, therefore, its use in single-electron memory might erode VUC advantage. To overcome this, the proposed scheme is combined with three-dimensional selection arrangement, which allows us to share the same word line between pair data lines. This is because the upper/lower selector cut off the data-line current drive of the spouse cell, while dummy cell is driving the spouse global data line. Due to this architecture, the area penalty due to the folded data line is negligible. By controlling the upper/lower selector in a time-multiplexed manner, a global data line and a sense amplifier is shared by upper and lower cells.

Using these techniques, an experimental 128-Mbit (8192 $\times$ 8192 $\times$ 2) memory is designed and fabricated. Although the memory cell is based on 0.25-μm technology, the cell size is as small as 0.145 μm^2/bit, which is close to the effective cell size of the 4-Gbit DRAM published at ISSCC97 [47]. A local data line is shared by 64 cells and, therefore, one block, upper and lower local data lines, includes 128 cells. One global data line is shared by 128 blocks. Read, write, and erase are simultaneously done using a word-line as the basic unit, which consists of 8000 cells. All the data are transferred serially by the four set of shift registers. The peripheral circuits use 0.4-μm CMOS technology, except the high-voltage transistors for write/erase use 1-μm channel length. The chip photograph is shown in Fig. 24, the operating waveform is shown in Fig. 25, the block diagram is shown in Fig. 26, and the design summary is show in Table 1.

Although all the operations are verified before fabrication using SPICE simulation, there were unexpected deviations from the design. The experimental read access time, 1.2 μs, is shorter than our design target, 20 μs, however, this is because we had to activate the sense amplifier earlier than the target timing due to the unexpected current leakage problem. We had a severe metal two short-circuit current problem, which is presumably due to metal dry-etching trouble (this type of trouble that often occurs in the experimental laboratory line, which is not the manufacturing line), and the portion of measurable part is very limited.



(a)

(b)

Fig. 24. (a) Microphotograph of 128-Mbit memory and (b) cross-sectional view of the memory array. In (b), double-stacked data lines and a source line are seen.

The operation waveform in Fig. 25 was taken in such a fortunate portion of the chip. Roughly half of the cells, even on the best wafer, show no current (this is measured on a smaller array, which does not suffer from the above etching problem). This is because the deposition condition of nano-Si film on a vertical surface was not well established for this first lot of the chip. The deposition thickness appears to be less than that on planer surface. In contrast, in a planer 8 $\times$ 8 array in Section IV, almost all cells worked if we ignore the threshold voltage variations.

VII. Conclusions

Single-electron memory as an integrated-circuit device is the subject of this paper. Only five years ago, single-electron phenomena were actively discussed in the physicist community, and the major source of the leading-edge research was *Physical Review Letters*. Now, the integrated-circuit device engineers are interested in the development of this new technology and the leading-edge source has moved to ISSCC and IEDM. Although these rapid advances—including LSI—have been made, we still are a long way from achieving gigascale integration and from the target that it be used in our pockets to store a variety

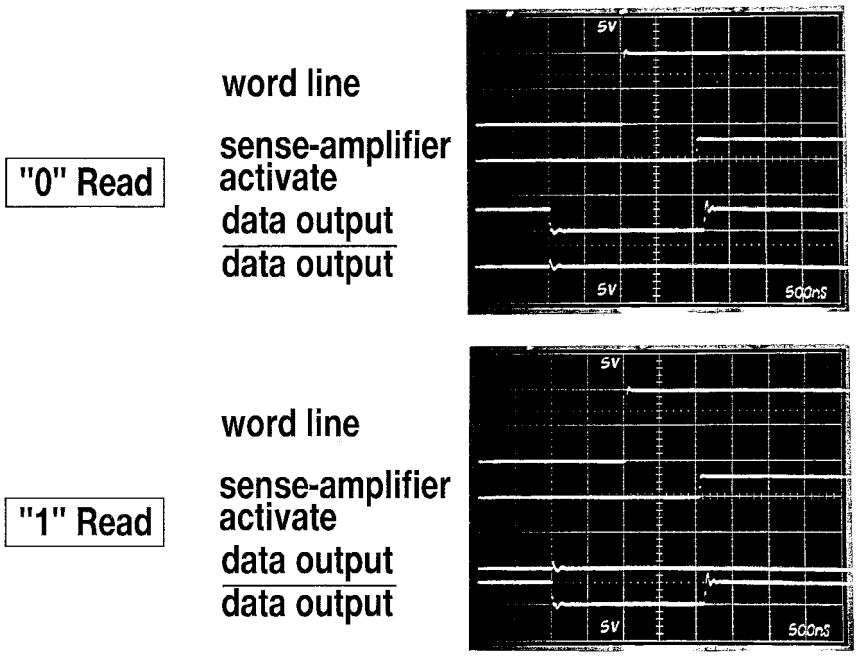


Fig. 25. Readout operating waveform of the memory prototype for both data 1 and 0.

of digital information. To conclude this article, remaining issues and questions are discussed.

We have relied heavily on the naturally formed nano-Si structures to make the above rapid progresses. However, it is not clear whether we should continue with this technology in the future. Recent demonstrations using more artificially defined structures [22]–[24] show much promise in this direction, whereas the strength of the naturally formed memory is (on the other hand) emphasized especially when we objectively compare the measured characteristics. Tiwari's device [22] stays somewhere between, and more study should be conducted.

The key to achieving the manufacturable single-electron device is the suppression of the cell-to-cell variations. More extensive study of the device structure and fabrication process is required. More advanced variation-compensation circuits and memory array organizations are also very important subjects for this purpose.

Although the advantage of the single-electron memory over conventional memories was intentionally narrowed to low bit-cost in our 128-Mbit prototyping, broader examinations should be made. A complementary scenario may focus on read/write speed, which apparently requires a significantly different cell structure than ours. Comparison to DRAM is important is this direction. This type of argument requires a wider range of expertise than currently involved in this field; for an introduction to scaling of memories, see van der Wagt's paper in this issue [48]. More system designers should be involved to make progress.

The single-electron memory as the superscalable device should be more thoroughly investigated, both theoretically and experimentally. Does the device have clear scalability advantage over conventional DRAM's or flash memories? This is still an open question.

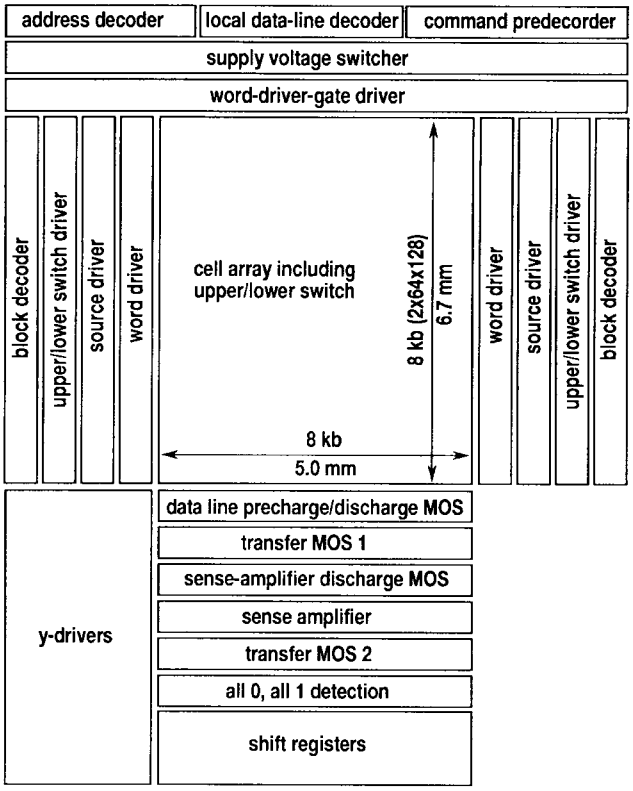


Fig. 26. Block diagram of the fabricated 128-Mbit memory prototype.

The digital-information storage era has just begun, and the need for the low-cost low-power memory technology should increase as time proceeds. It has yet to be clarified whether the single-electron memory will become the key device in this era. However, the challenges are becoming more and more concrete and are waiting to be tackled.

Table 1
Design Summary of 128-Mbit Memory Prototype

Technology	0.25 μm Cell + 0.4μmCMOS n+ poly-Si gate, LOCOS 2-level Metal (Al/W)
Gate Oxide	25 nm
Gate Length	0.4 μm 1.0 μm (high voltage)
Cell Size	0.5 μm x 0.58 μm/2bits
Architecture	vertically unified cells hierarchical folded data line
Read (first)	20 μs
(serial)	10 ns cycle time
Store/Clear	100 μs/sector (typical)
Chip Size	5.0 mm x 6.7 mm (memory array) 10.28 mm x 8.55 mm(total including pads)

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REFERENCES

[1] D. V. Averin and K. K. Likharev, in *Quantum Effects in Small Disordered Systems*, B. Al'tshuler *et al.*, Eds. London, U.K.: Elsevier, 1991.

[2] K. K. Likharev, in *Granular Nanoelectronics*, D. K. Ferry, J. R. Baker, and C. Jacoboni, Eds. New York: Plenum, 1991.

[3] H. Grabert and M. H. Devoret, Eds., "Single-charge tunneling," *NATO ASI Series B.* New York: Plenum, 1991.

[4] T. A. Fulton and G. J. Dolan, "Observation of single-electron charging effects in small tunnel junctions," *Phys. Rev. Lett.*, vol. 59, no. 1, pp. 109–112, July 1987.

[5] L. S. Kuzmin and K. K. Likharev, *JETP Lett.*, vol. 45, no. 8, pp. 495–497, 1987.

[6] U. Meirav, M. Kastner, and S. J. Wind, "Single-electron charging and periodic conductance resonances in GaAs nanostructures," *Phys. Rev. Lett.*, vol. 65, no. 6, pp. 771–774, Aug. 1990.

[7] L. J. Geerligs, V. F. Andregg, P. A. Holweg, J. E. Mooij, H. Pothier, D. Esteve, C. Urbina, and M. H. Devoret, "Frequency-locked turnstile device for single-electrons," *Phys. Rev. Lett.*, vol. 64, no. 22, p. 2691, May 1990.

[8] L. P. Kouwenhoven, A. T. Johnson, N. C. van der Vaart, C. J. P. M. Harmans, and C. T. Foxon, "Quantized current in a quantum-dot turnstile using oscillating tunnel barriers," *Phys. Rev. Lett.*, vol. 67, no. 12, p. 1626, Sept. 1991.

[9] T. A. Fulton, P. L. Gammel, and L. N. Dunkleberger, "Determination of Coulomb-blockade resistances and observation of the tunneling of single electrons in small-tunnel-junction circuits," *Phys. Rev. Lett.*, vol. 67, no. 22, p. 3148, Nov. 1991.

[10] K. Nakazato, R. J. Blaikie, J. R. Cleaver, and H. Ahmed, "Single-electron memory," *Electron. Lett.*, vol. 29, no. 4, p. 384, 1993.

[11] K. Nakazato and H. Ahmed, *Adv. Mater.*, vol. 5, no. 9, p. 668, 1993.

[12] K. Nakazato, R. J. Blaikie, and H. Ahmed, *J. Appl. Phys.*, vol. 75, no. 10, p. 5123, May 1994.

[13] K. Yano, T. Ishii, T. Hashimoto, T. Kobayashi, F. Murai, and K. Seki, "Room-temperature single-electron memory using fine-grain polycrystalline silicon," in *Proc. IEEE Int. Electron Devices Meeting*, 1993, pp. 541–545.

[14] ——, "Room-temperature single-electron memory," *IEEE Trans. Electron Devices*, vol. 41, pp. 1628–1638, 1994.

[15] K. Yano, T. Ishii, T. Sano, T. Mine, F. Murai, and K. Seki, "Single electron-memory integrated circuit for giga-to-tera bit storage," in *Proc. 1996 IEEE Int. Solid-State Circuits Conf.*, 1996, pp. 266–267.

[16] R. C. Ashoori, "Electrons in artificial atoms," *Nature*, vol. 379, pp. 413–419, 1996.

[17] K. K. Likharev, "Correlated discrete transfer of single electrons in ultrasmall tunnel junctions," *IBM J. Res. Develop.*, vol. 32, no. 1, pp. 144–158, 1988.

[18] D. A. Averin and K. K. Likharev, "Possible applications of the single-charge tunneling," in *Single-Charge Tunneling* (NATO ASI Series B.), H. Grabert and M. H. Devoret, Eds. New York: Plenum, 1991.

[19] M. Akazawa and Y. Amemiya, "Boltzmann machine neuron circuit using single-electron tunneling," *Appl. Phys. Lett.*, vol. 70, no. 5, pp. 670–672, 1997.

[20] N. Asahi, M. Akazawa, and Y. Amemiya, "Binary-decision diagram device," *IEEE Trans. Electron Devices*, vol. 42, pp. 1999–2003, Nov. 1995.

[21] V. P. Roychowdhury, D. B. Janes, and S. Bandyopadhyay, "Nanoelectronic architecture for Boolean logic," *Proc. IEEE*, vol. 85, pp. 574–588, Apr. 1997.

[22] S. Tiwari, F. Rana, K. Chan, H. Hanafi, W. Chan, and D. Buchanan, "Volatile and nonvolatile memories in silicon with nano-crystal storage," in *Proc. IEEE Int. Electron Devices Meeting*, 1995, pp. 521–524.

[23] A. Nakajima, T. Futatsugi, K. Kosemura, T. Fukano, and N. Yokoyama, "Room-temperature operation of Si single-electron memory with self aligned floating dot gate," *Proc. IEEE Int. Electron Devices Meeting*, 1996, pp. 952–954.

[24] L. Guo, E. Leobandung, and S. Y. Chou, "Si single-electron MOS memory with nanoscale floating-gate and narrow channel," *Proc. IEEE Int. Electron Devices Meeting*, 1996, pp. 955–956.

[25] J. Lambe and R. C. Jaklevic, "Charge-quantization studies using tunnel capacitor," *Phys. Rev. Lett.*, vol. 22, no. 25, pp. 1371–1375, June 1969.

[26] D. V. Averin and K. K. Likharev, "Possible coherent oscillations at single-electron tunneling," in *Proc. SQUID '85*, Berlin, p. 197.

[27] ——, "Coulomb blockade of the single-electron tunneling and coherent oscillations in small tunnel junctions," *J. Low Temp. Phys.*, vol. 62, p. 345, 1986.

[28] K. K. Likharev, "Single-electron transistors: Electrostatic analogs of the DC SQUID's," *IEEE Trans. Magnetics*, vol. 23, p. 1142, Mar. 1987.

[29] D. Esteve, "Transferring electrons one by one," in *Single-Charge Tunneling* (NATO ASI Series B), H. Grabert and M. H. Devoret, Eds. New York: Plenum, 1991.

[30] P. Delsing, "One-dimensional arrays of small tunnel junctions," in *Single-Charge Tunneling* (NATO ASI Series B), H. Grabert and M. H. Devoret, Eds. New York: Plenum, 1991.

[31] P. D. Dresselhaus, L. Ji, S. Han, J. E. Lukens, and K. K. Likharev, "Measurement of single-electron lifetimes in a multi-junction trap," *Phys. Rev. Lett.*, vol. 72, no. 20, pp. 3226–3229, May 1994.

[32] C. Schönenberger and H. van Houten, in *Proc. 1992 Int. Conf. Solid State Devices and Materials*, 1992, p. 726.

[33] M. J. Kirton and M. J. Uren, "Noise in solid-state microstructures: A new perspective on individual defects, interface states and low-frequency (l/f) noise," *Adv. Physics*, vol. 38, p. 367, 1989.

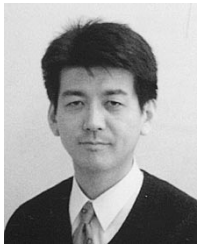
[34] K. Yano, T. Ishii, T. Hashimoto, T. Kobayashi, F. Murai, and K. Seki, "Transport characteristics of polycrystalline-silicon with influenced by single electron charging at room temperature," *Appl. Phys. Lett.*, vol. 67, no. 6, pp. 828–830, Aug. 1995.

[35] K. Yano, T. Ishii, T. Sano, T. Mine, F. Murai, and K. Seki, "Synchronous single-electron transfer at room temperature," in *Quantum Coherence and Denoherence*, K. Fujikawa and Y. A. Ono, Eds. London, U.K.: Elsevier, 1996.

[36] K. Nakazato and H. Ahmed, "Enhancement of coulomb blockade," *Appl. Phys. Lett.*, vol. 66, no. 23, pp. 3170–3172, June 1995.

[37] Y. Takahashi, M. Nagase, H. Namatsu, K. Kurihara, K. Iwdate,

Y. Nakajima, S. Horiguchi, K. Murase, and M. Tabe, "Conductance oscillations of a Si single electron transistor at room temperature," in *Proc. IEEE Int. Electron Devices Meeting*, 1994, pp. 938–940.
[38] K. Matsumoto, M. Ishii, K. Segawa, Y. Oka, B. J. Vartanian, and J. S. Harris, "Room temperature operation of single electron transistor made by STM nano-oxidation process," in *Ext. Abstr. 1995 Int. Conf. Solid State Devices and Materials*, Osaka, Japan, 1995, pp. 192–194.
[39] K. Yano, T. Ishii, T. Sano, T. Mine, F. Murai, T. Kure, and K. Seki, "A 128-Mb early prototype for gigascale single-electron memories," in *Proc. 1998 IEEE Int. Solid-State Circuits Conf.*, to be published.
[40] K. Yano, T. Ishii, T. Sano, T. Mine, F. Murai, and K. Seki, "Impact of Coulomb blockade on low-charge limit of memory device," in *Proc. IEEE Int. Electron Devices Meeting*, 1995, pp. 525–528.
[41] T. Ishii, K. Yano, T. Sano, T. Mine, F. Murai, and K. Seki, "Verify: Key to the stable single-electron memory operation," in *Proc. IEEE Int. Electron Devices Meeting*, 1997, pp. 171–174.
[42] K. K. Likharev and A. N. Korotkov, "Ultradense hybrid SET/FET dynamic RAM: Feasibility of background-charge-independent room-temperature single-electron digital circuits," submitted for publication.
[43] T. Ishii, K. Yano, T. Sano, T. Mine, F. Murai, and K. Seki, "3-D single-electron memory cell with 2F2 per bit," in *Proc. IEEE Int. Electron Devices Meeting*, 1997, pp. 924–926.
[44] V. N. Kynett, A. Baker, M. L. Fandrich, G. P. Hoekstra, O. Jungroth, J. A. Kreifels, S. Wells, and M. D. Winston, "An in-system reprogrammable 32K×8 CMOS flash memory," *IEEE J. Solid-State Circuits*, vol. 23, p. 1157, Oct. 1988.
[45] K. Seki, H. Kume, Y. Ohji, T. Kobayashi, A. Hiraiwa, T. Nishida, T. Wada, K. Komori, K. Izawa, T. Nishimoto, Y. Kubota, and K. Shoji, "An 80-ns 1-Mb flash memory with on-chip erase/erase-verify controller," *IEEE J. Solid-State Circuits*, vol. 25, p. 1147, Oct. 1990.
[46] K. Itoh, "Trends in megabit DRAM circuit design," *IEEE J. Solid-State Circuits*, vol. 25, p. 778, 1990.
[47] T. Murotani *et al.*, in *Proc. IEEE Int. Solid-State Circuits Conf.*, 1997, p. 74.
[48] J. P. A. van der Wagt, "Tunneling-based SRAM," this issue, pp. 571–595.
[49] P. D. Tougaw and C. S. Lent, "Logical devices implemented using quantum cellular automata," *J. Appl. Phys.*, vol. 75, no. 3, pp. 1818–1825, Feb. 1994.
[50] T. Ohshima and R. A. Kiehl, "Operation of bistable phase-locked single electron tunneling logic elements," *J. Appl. Phys.*, vol. 80, pp. 912–923, 1996.
[51] K. K. Likharev, "Single-electron devices and their applications," this issue, pp. 606–632.



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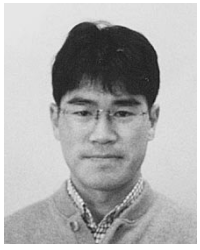

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