Double-Gate Strained-Ge Heterostructure Tunneling FET (TFET) With Record High Drive Currents and <60mV/dec Subthreshold Slope

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Abstract

The main challenges for Tunnel FETs are experimentally demonstrating SS<60mV/dec, high ON currents and solving their ambipolar behavior. We have experimentally demonstrated a Double-Gate, Strained-Ge, Heterostructure Tunneling FET (TFET) exhibiting very high drive currents and SS<60mV/dec. Due to small bandgap of s-Ge and the electrostatics of the DG structure, record high drive current of 300uA/um (the highest ever reported experimentally for a TFET) and a subthreshold slope of ~50mV/dec was observed.

In addition, to address the ambipolar problem and examine the scalability of TFETs, we have developed a sophisticated TFET simulator that uses a Quantum transport model, Non-local BTBT, complete Bandstructure (real and complex) information, and includes all transitions (direct and phonon assisted). Using this simulator, we have studied the scalability of three asymmetric DG TFET configurations (underlapped drain, lower drain doping and lateral heterostructure) in terms of their ability to solve the ambipolar behavior and achieve high ON and low OFF currents.

Introduction

As we scale down MOSFETs to the nanoscale, power dissipation is a huge concern. Lowering the supply voltage (Vdd) is very difficult due to the exponentially increasing sub-threshold leakage, which follows a transport mechanism governed by carrier diffusion over a thermal barrier, and is limited to 60mV/dec turn-off in the best case. In order to allow supply voltage reduction, novel transistor structures need to be investigated [1-3]. One such transistor structure is the TFET, where the transport is dictated by tunneling through a source barrier (instead of diffusion over the barrier). Many recent studies have been performed investigating different TFET structures [4-9]. However, one big concern with TFETs is that they may not exhibit high drive currents due to a high tunneling resistance. We have experimentally demonstrated s-Ge, DG TFETs exhibiting record high drive currents, almost comparable to conventional MOS, showing that the a small bandgap material can significantly reduce the tunnel resistance.

Another problem with TFETs is that they exhibit ambipolar behavior, which leads to high off-state leakage. We have developed a TFET simulator that uses a Quantum transport model, Non-local BTBT, complete Bandstructure information, and includes all transitions. Using this simulator, we have studied the scalability of three asymmetric DG TFET configurations, in their ability to solve the ambipolar problem and achieve high ON-currents and low OFF-leakage.

Device structure (Experimental)

Fig 1 shows (a) the schematic the s-Ge heterostructure TFET that was fabricated on an UT-SOI substrate, (b) the band-diagram and (c) the cross-sectional TEM showing the different layers. The fabrication process is similar to that described in [10] except that the source and drain are doped p+ and n+. Low temperature deposited oxide was used to prevent the s-Ge from relaxing and to obtain low gate leakage.

Strained-Ge Double-Gate Tunnel FETs (Experimental)

Fig. 2 shows a schematic of a TFET with either large bandgap (Eg) material (Si) or small Eg material (s-Ge) as the channel. The working of the TFET is described in Fig. 3 (a) ON-state (b) Min, IOFF-state (c) AMBIPOLAR-state. A small Eg channel material, like s-Ge has much larger tunneling currents (in both, ON and OFF-state) compared to a large Eg material like Si. Fig. 4 is the experimental Id-Vg characteristic of a control single-gate (SG) Si TFET. The Ion saturates at ~10-100nA/um due to the large (and indirect) Eg of Si ~1.1eV, which leads to a large tunnel resistance. Fig. 5 is the experimental Id-Vg characteristic of a SG s-Ge TFET. The Ion is very high ~100uA/um and due to the extremely small Eg of s-Ge ~0.4eV [11].

In addition, we also fabricated s-Ge heterostructure TFETs on UT-SOI, and measured them in a "Double-Gate" configuration by using bank-gate bias on the substrate (Fig. 6). Fig. 7 is the corresponding experimental Id-Vg characteristic. Due to small Eg of s-Ge and the electrostatics of the DG structure the drive currents are a record 300uA/um, which is the highest ever reported experimentally (Table 1) for a TFET and almost comparable to conventional MOS. The device also exhibits a best observed SS of ~50mV/dec.

TFET Ambipolar problem and Scalability (Simulation)

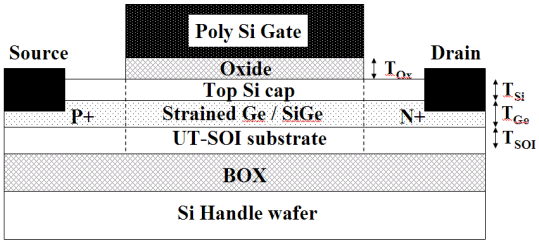
We have developed a TFET simulator that uses a Non-local BTBT model, Quantum transport, complete Bandstructure (real and complex), and includes all transitions (direct and phonon assisted). The simulated s-Ge DG TFET characteristics in Fig. 7(b) match the experimental data in Fig. 7(a) very well. In order to solve the ambipolar behavior in TFETs, asymmetry must be introduced between Source and Drain (Fig. 8). Using our TFET simulator, we have studied the scalability of (A) Symmetric and three asymmetric DG TFET configurations (Fig. 9), (B) Underlap drain, (C) Low drain-doping and (D) Lateral heterostructure in their ability to solve the ambipolar problem and achieve high ON and low OFF currents. Fig. 10-11 show that increasing the drain underlap from 0-40nm and lowering the drain doping from 1e20-1e18cm^{-3} can kill the ambipolar behavior. However, Fig. 12 shows that both these approaches are not fundamentally different and both lower leakage due to a long depletion width and low E-field on the drain side. Unfortunately, both these TFET structures need a very long NON-scaling Drain of >30nm to achieve a SS<60mV/dec. This puts a severe restriction on device scalability. The ambipolar problem can also be solved using a lateral heterostructure of a large Eg material (like Si) at the drain side (Fig. 13) to reduce the tunneling. Fig. 14 shows that a Source-Side heterostructure can effectively solve the ambipolar problem (Fig. 15). The lateral heterostructure is the most scalable approach to solving the ambipolar problem (Fig. 9.)

Conclusion

We have experimentally demonstrated a DG, s-Ge, TFET exhibiting record Ion (~300uA/um) and SS~50mV/dec. Using our novel TFET simulator, we also show that the lateral heterostructure is the most effective and scalable approach to solve the ambipolar issue in TFETs.

References

[1]Salahuddin et al, arxiv, 0707.2073, 2073. [2]Gopalakrishnan et al, IEDM, p.289, 2002.[3]Akarvardar et al, TED, 2008. [4]Appenzeller, PRL 93, 196805, 2004. [5]Bhuwalka et al, TED,51,2,p.279,2004. [6] Reddick et al, APL, 67 (4), 1995 [7]Choi et al, EDL, p.743, 2007. [8] Nirschl et al, IEEE ISCAS, p.713 2004 [9]P. wang et al, SSE, 48, p.2281, 2004. [10]T. Krishnamohan et al, VLSI Symp. p.82, 2005. [11]T. Krishnamohan et al, TED p.990, May 2006.



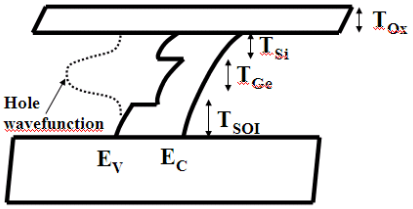


Fig. 1 (a) and (b): Schematic of the (a) cross-section of Strained-Ge Heterostructure TFET on UTSOI that was fabricated and (b) Band diagram of the strained-Ge Heterostructure TFET

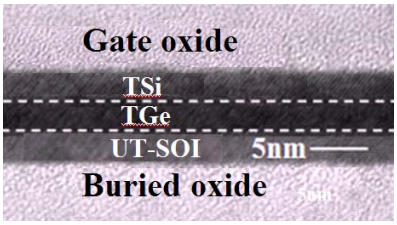


Fig. 1 (c): Cross-sectional TEM of Strained-Ge Heterostructure TFET on UTSOI that was fabricated

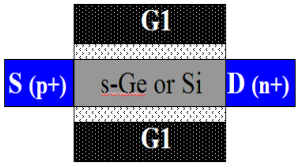


Fig. 2: Schematic of the Double-Gate TFET device structure with Si and s-Ge channel

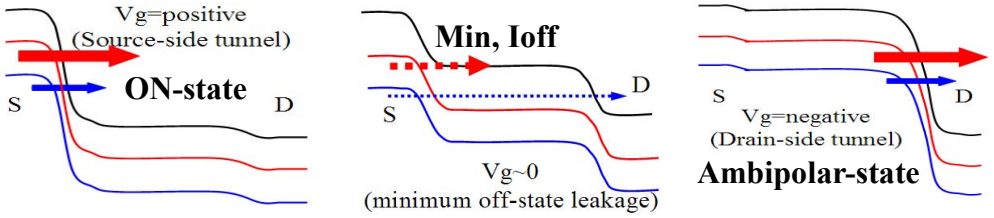


Fig. 3: Band-diagram of the DG TFET at different Vg bias. (a) ON-state (b)Min, Ioff point (c) OFF-state. A small bandgap channel material, like s-Ge has much larger tunneling currents (in both, ON and OFF-state) compared to a large bandgap material like Si.

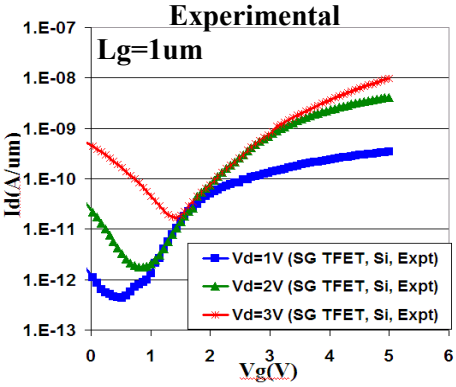


Fig. 4: Experimental Single-Gate Silicon NMOS TFET. Si channel shows Very low ION and IOFF due to large bandgap.

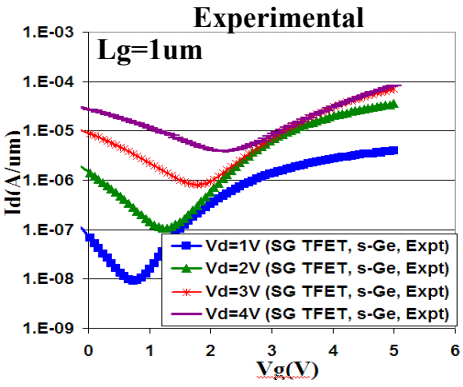


Fig. 5: Experimental Single-Gate s-Ge TFET. Straind-Ge shows high ION but high IOFF due to small bandgap.

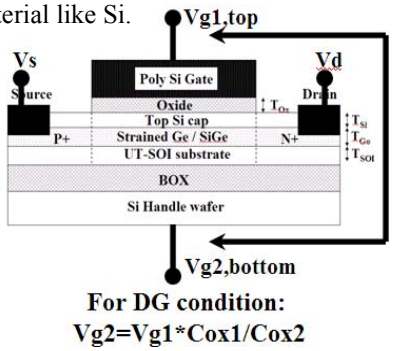


Fig. 6: Experimental bias setup condition for creating a "Double-Gate" FET using appropriate back-gate bias on the substrate/BOX of and UT-SOI FET.

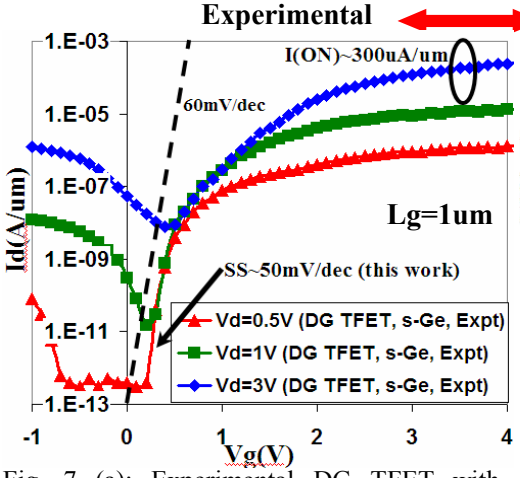


Fig. 7 (a): Experimental DG TFET with strained-Ge heterostructure channel shows record high drive currents (Ion~300uA/um) and good SS~50mV/dec, due to small bandgap of s-Ge and DG electrostatics

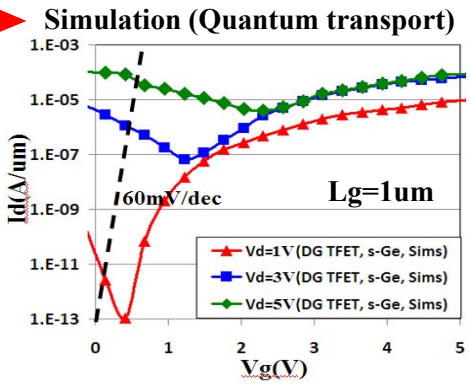


Fig. 7 (b): We have developed a TFET simulator that uses a Non-local BTBT model, Quantum transport, complete Bandstructure (real and complex), and all transitions (direct and phonon assisted). Simulated s-Ge DG TFET characteristics match experimental data [7(a)] very well.

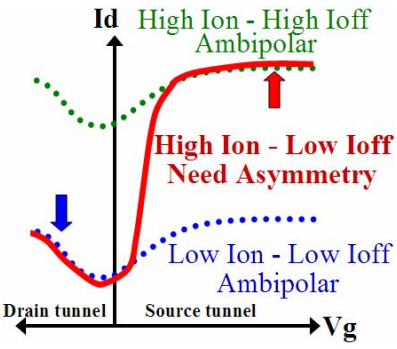


Fig. 8: Symmetric TFETs exhibit ambipolar characteristics. Asymmetry must be introduced in the structure between Source-side tunneling and Drain–side tunneling in order to achieve high ON and low OFF currents.

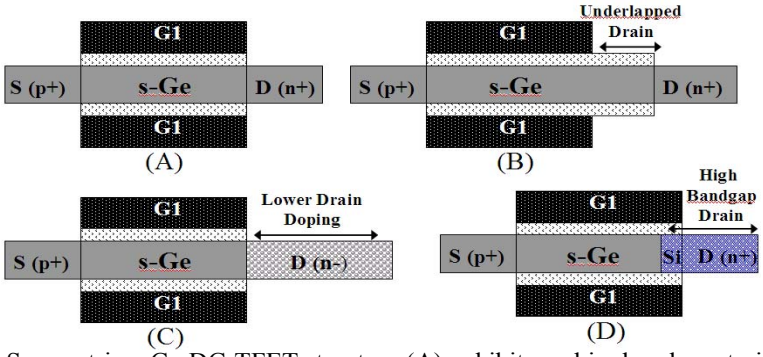


Fig. 9: Symmetric s-Ge DG TFET structure (A) exhibits ambipolar characteristics (See Fig. 7). In order to achieve high ON and low OFF, asymmetry can be introduced into the TFET by (B) using an under-lapped drain, or (C) using a lower doping on the drain side, or (D) using a lateral heterostructure of large bandgap material (like Si) to reduce the tunneling currents from the drain during OFF-state.

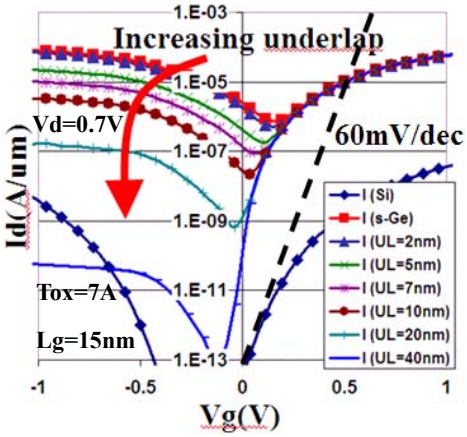


Fig. 10: **Asymmetry by Increasing underlap:** The effect of increasing the drain underlap on the leakage of the TFET. Simulations show that a very large underlap of ~40nm is needed to achieve a sub-threshold slope <60mV/dec.

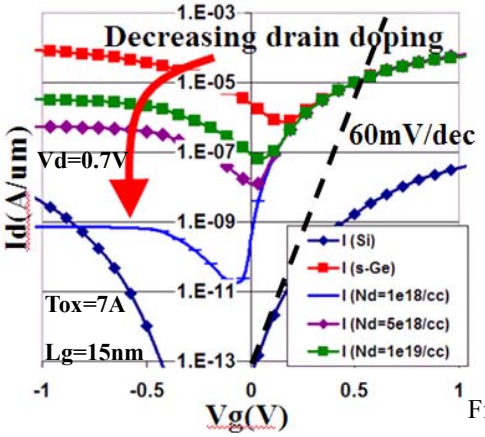


Fig. 11: **Aymmetry by Lower Drain-Doping:** The effect of lowering the drain doping on the leakage of the TFET. Simulations show that a very low doping of ~1e18/cc is needed to achieve a SS<60mV/dec.

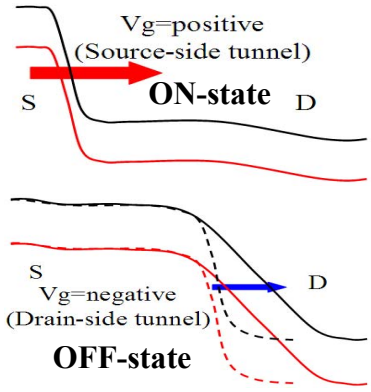


Fig. 12: Fundamentally, underlapped gate (Fig 9-B) and low-drain doping (Fig.9-C) are not different. Both lower leakage due to a long depletion width with low E-field on the drain side. Both these TFET structures need a very long NON-scaling Drain length of ~40nm,

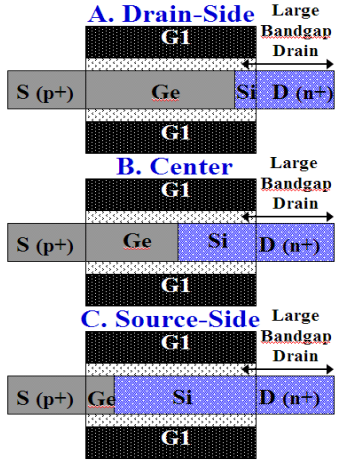


Fig. 13: **Asymmetry by Lateral Heterostructure:** Solving the ambipolar problem by using a large bandgap material (Si) at the drain side to reduce the tunneling. Different locations of the s-Ge/Si interface.

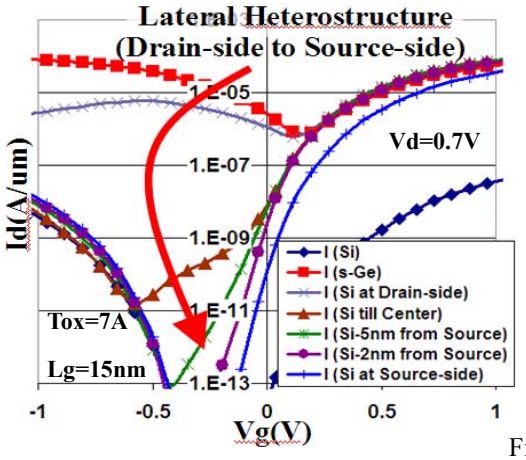


Fig. 14: The effect of the location of the s-Ge/Si interface on the leakage of the lateral heterostructure TFET. Simulations show that a Source-Side heterostructure (interface between s-Ge and Si is at the source-side) is needed to achieve a SS<60mV/dec.

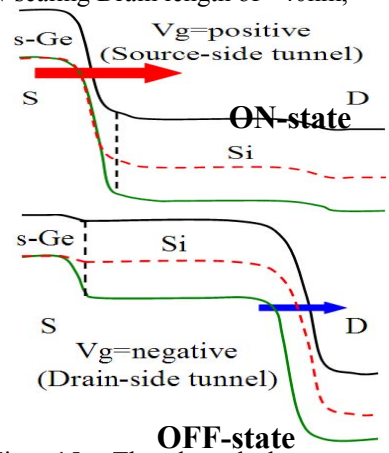


Fig. 15: The lateral heterostructure TFET (Fig. 13-C) with s-Ge/Si interface at the Source-side can significantly suppress the drain side tunneling during OFF-state due to the large bandgap of Si (compared to Ge), while maintaing high drive currents in ON-state.

Reference TFETs (experimental)	I(ON) (uA/um)	SS (mV/dec)
This work (expt.)	~300	~50
[4] Appenzeler (expt.)	<0.01	~40
[5] Bhuwalka (expt.)	~0.1	>300
[6] Reddick (expt.)	~0.1	>400
[7] Choi (expt.)	~1	~50
[8] Nirschl (expt.)	~1	>300
[9] Wang (expt.)	~3	~100

Table 1: Comparison of different experimental TFET structures. The TFET reported in this paper exhibits the highest drive current and SS<60mV/dec.