Comparison of graded and abrupt junction $In_{0.53}Ga_{0.47}As$ heterojunction bipolar transistors

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We compare calculated intrinsic forward delay as a function of base thickness and p-type doping level in n-p-n heterojunction bipolar transistors with graded as well as abrupt $Al_{0.48}In_{0.52}As/In_{0.53}Ga_{0.47}As$ and $InP/In_{0.53}Ga_{0.47}As$ emitter-base junctions. We find that, for a given p-type concentration and fixed base delay time, an $InP/In_{0.53}Ga_{0.47}As$ abrupt junction design results in high intrinsic speed, low base resistance, and modest power consumption.

Much progress has been made fabricating high speed n-p-n heterojunction bipolar transistors (HBTs) lattice matched to InP. Very high speed circuits have been demonstrated (Ref. 1) as well as discrete devices (Ref. 2). There has, however, been little attempt to optimize and quantify the intrinsic merits of various transistor designs.

We present results of numerically simulating charge transport in graded and abrupt junction n-p-n HBTs lattice matched in InP. We find that base resistance may be minimized by making use of an abrupt emitter-base junction which has a conduction band offset resulting in extreme nonequilibrium transport in the base. However, high energy injection is obtained at the cost of larger turn-on voltage in abrupt compared to graded junction HBTs. This is particularly true for the $Al_{0.48}In_{0.52}As/In_{0.53}Ga_{0.47}As$ heterojunction which has a large conduction band offset $\Delta E_C = 0.47$ eV. Hence, power consumption in a typical digital circuit is best minimized using devices with a graded emitter-base junction which have a low V_{BE} turn-on voltage. These devices require a shorter and more heavily doped base than an abrupt junction HBT, as well as a more complex crystal growth sequence necessary to achieve grading. Overall, we find that a simple abrupt $InP/In_{0.53}Ga_{0.47}As$ emitter-base junction results in a good design compromise by combining low power consumption with a very impressive subpicosecond intrinsic high speed response.

The inset in Fig. 1(a) shows a schematic band diagram of a typical $Al_{0.48}In_{0.52}As/In_{0.53}Ga_{0.47}As$ n-p-n HBT under forward bias. The Γ-valley conduction band minimum CB_{min}, the subsidiary conduction band L-minimum, and the valence band maximum VB_{max}, are indicated. The base has thickness x_B and the collector space-charge region has thickness x_C. The large conduction band off-set $\Delta E_C = 0.47$ eV between the $Al_{0.48}In_{0.52}As$ emitter and the $In_{0.53}Ga_{0.47}As$ base results in extreme nonequilibrium electron transport phenomena in the base which dramatically influences the static (Ref. 3) and dynamic (Ref. 4) characteristics of the device. Qualitatively, we expect such nondiffusive electron transport
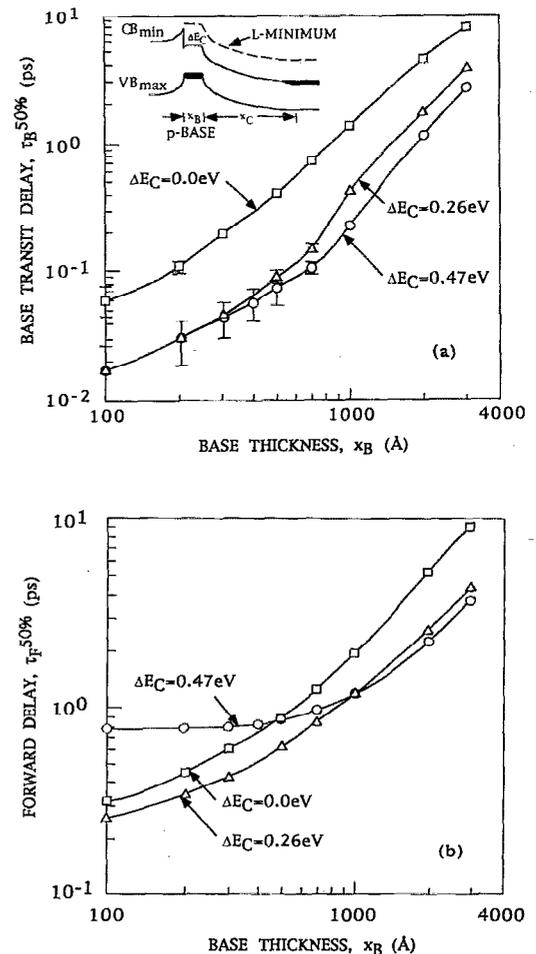

FIG. 1. (a) Delay, $\tau_B^{50\%}$, for different base thicknesses, x_B and the indicated values of ΔE_C. The simulation is for HBTs with base doping $p=1\times10^{19}$ cm^{-3} operated at temperature $T=300$ K, current density 5×10^4 A cm^{-2}, $x_C=3000$ Å, the collector space-charge region is doped $n=2\times10^{16}$ cm^{-3}, and collector-base voltage $V_{CB}=0.25$ V. The inset shows a schematic band diagram of an abrupt junction n-p-n $Al_{0.48}In_{0.52}As/In_{0.53}Ga_{0.47}As$ HBT under forward bias. (b) Results of calculating $\tau_F^{50\%}$, as a function of x_B and ΔE_C for the same device as in (a).

to provide a design window in which base thickness may be increased to reduce base resistance without significantly sacrificing intrinsic forward delay time.

To quantify these ideas we performed numerical simulations of electron transport in HBTs with different conduction band offsets ΔE_C, base thickness x_B, and different p-type impurity concentration in the base. In our model, initially, a thermal distribution of electrons in the forward biased wide band gap emitter-base junction are injected with approximate excess kinetic energy ΔE_C ($\Delta E_C = 0$ eV for graded emitter) into the Γ-valley conduction band of the p-type $In_{0.53}Ga_{0.47}As$ base. For large ΔE_C, some fraction of electrons enter the base, or subsequently scatter, into the subsidiary L valley 0.55 eV above CB_{min} [see inset Fig. 1(a)]. We take into account elastic and inelastic electron scattering processes such as electron–electron, electron–phonon, and intervalley transfer. Electron transfer from the nonparabolic Γ valley to the high effective electron mass L- and X-valley conduction band minima are particularly important in the reverse biased collector space-charge region. Our model determines electron trajectories using a semiclassical Monte Carlo algorithm (Refs. 5–7) in which Poisson's equation is satisfied throughout the simulation.

In Fig. 1(a) we plot results of calculating base transit delay, $\tau_B^{50\%}$, for 50% of step-injected emitter current to flow through the base. The simulation is for a HBT operated at temperature $T = 300$ K, with an $In_{0.53}Ga_{0.47}As$ base doped $p = 1 \times 10^{19}$ cm^{-3}, current density $j = 5 \times 10^4$ A cm^{-2}, $x_C = 3000$ Å, $In_{0.53}Ga_{0.47}As$ collector space-charge region doped $n = 2 \times 10^{16}$ cm^{-3}, and collector-based voltage $V_{CB} = 0.25$ V. The three $\tau_B^{50\%}$ vs x_B curves are for $\Delta E_C = 0.47$ eV, $\Delta E_C = 0.26$ eV, and $\Delta E_C = 0$ eV corresponding to an abrupt $Al_{0.48}In_{0.52}As$, InP and graded emitter, respectively. The numerical simulations show that $\tau_B^{50\%}$ can be maintained at a small value for a wider range of x_B by using an abrupt emitter-base junction with large ΔE_C. This result is a direct consequence of the existence of extreme nonequilibrium transport in the transistor base for devices with large ΔE_C.

In Fig. 1(b) we show calculated forward delay $\tau_F^{50\%} = \tau_B^{50\%} + \tau_C^{50\%}$ as a function of base thickness for the same device designs as used in Fig. 1(a). Here we see the influence collector delay $\tau_C^{50\%}$ has on forward delay $\tau_F^{50\%}$. Devices with $\Delta E_C = 0.47$ eV have large $\tau_F^{50\%}$ for small x_B since, unlike a classical transistor in which base and collector charge transport are decoupled, nonequilibrium electron transport dynamics in the base can increase collector delay, $\tau_C^{50\%}$. This occurs because, for small x_B, electrons arrive at the base-collector junction with significant excess kinetic energy, are readily accelerated to high energies by the electric field in the collector space-charge region, and therefore efficiently scatter into low velocity L- and X-valley subsidiary minima. Under these circumstances, collector delay can be greater than in the corresponding diffusive device.

In Fig. 2 we illustrate this by plotting the steady-state Γ- and L-valley population as a function of position, x, in a device with $x_B = 400$ Å, $p = 1 \times 10^{19}$ cm^{-3}, and (a) $\Delta E_C = 0.47$ eV and (b) $\Delta E_C = 0$ eV. The high injection energy used for Fig. 2(a) results in a small number of electrons being introduced into the L valley. In addition, electrons
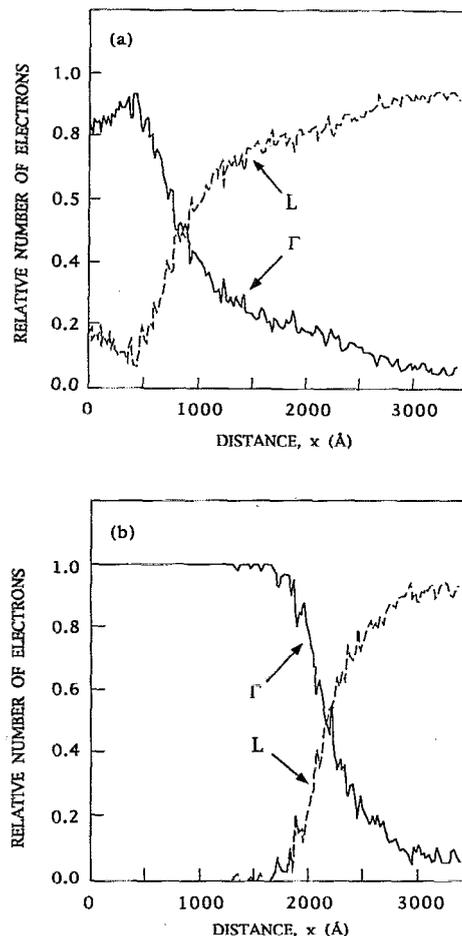

FIG. 2. Calculated steady-state Γ- and L-valley population as a function of distance, x, for device of Fig. 1 with $x_B = 400$ Å and (a) $\Delta E_C = 0.47$ eV, (b) $\Delta E_C = 0.0$ eV.

maintain their excess kinetic energy while traversing the thin base so that electrons accelerated in the collector space-charge region rapidly transfer into the low velocity L valley. By way of contrast, Fig. 2(b) shows that for $\Delta E_C = 0$ eV electrons remain in the high velocity Γ valley for most of the time while traversing the collector space-charge region of the device.

In Figs. 3(a) and 3(b) we show results of calculations similar to those used to generate Fig. 1 but now for HBTs with $p = 1 \times 10^{20}$ cm^{-3}. Clearly, the underlying trends established above are maintained for devices with an order of magnitude more p-type doping. There are, however, a number of small differences. For example, $\tau_F^{50\%}$ initially decreases with increasing x_B since slightly more efficient electron cooling in the base results in a reduced $\tau_C^{50\%}$.

Because minority carrier mobility in $In_{0.53}Ga_{0.47}As$ decreases sublinearly with increasing majority carrier concentration it is clear from the above that adopting high p-type doping levels is a good strategy to ensure both small $\tau_F^{50\%}$ and low base resistance in *any* of the transistor designs we have considered. However, the use of an abrupt $Al_{0.48}In_{0.52}As/In_{0.53}Ga_{0.47}As$ emitter-base junction allows for about a factor of two thicker base and lower base resistance
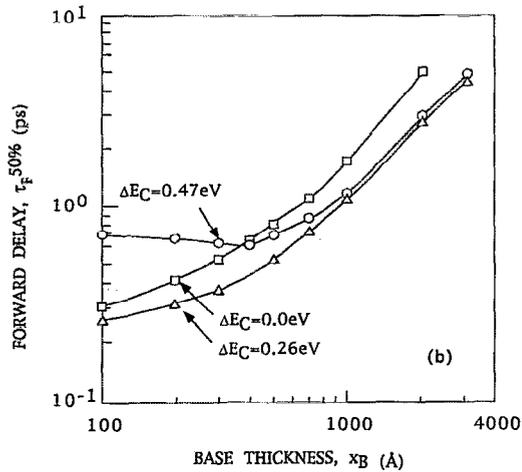
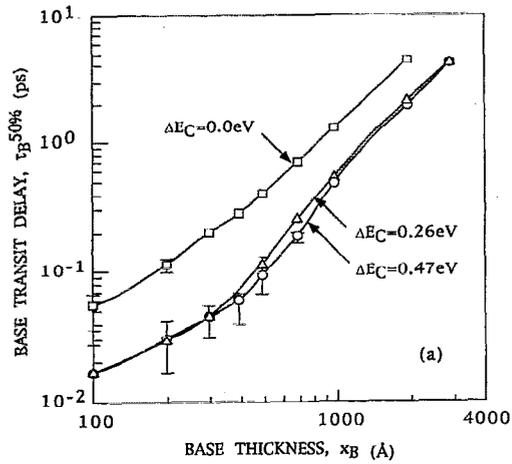FIG. 3. Same as Figs. 1(a) and 1(b) but for $p=1\times10^{20}$ cm^{-3}.

Emitter	$Al_{0.48}In_{0.52}As$	InP	Graded
V_{BE}(V)	1.2	0.9	0.7
V_{EE}(V)	−4.4	−3.5	−2.9
Relative power	1.0	0.79	0.66

this example. Obviously, a significant reduction in power dissipation can be achieved through the use of either an abrupt $InP/In_{0.53}Ga_{0.47}As$ or graded emitter-base junction compared to an abrupt junction $Al_{0.48}In_{0.52}As/In_{0.53}Ga_{0.47}As$ device. We note that a graded junction HBT has other advantages such as a large valence band offset and a low emitter dynamic resistance.

In conclusion, we have compared the relative merits of HBTs with various emitter-base junction designs. We find that, for a given base delay time, implementation of an abrupt junction allows use of a thicker base and thus lower base resistance compared to a graded junction. Since the abrupt junction increases the device turn-on voltage by approximately ΔE_C, the relatively small conduction band discontinuity of an abrupt junction $InP/In_{0.53}Ga_{0.47}As$ device represents a good compromise between high intrinsic speed, low base resistance, and reasonably low power consumption.

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compared to a graded device. Nevertheless, if the device is limited by resistive and capacitive parasitics, a graded emitter has important advantages for digital circuit applications. In Table I we list the turn-on voltage V_{BE}, minimum supply voltage V_{EE}, and normalized power dissipation for a series gated current mode logic (CML) latch which is the standard building block of many bipolar digital circuits. The minimum supply voltage in this architecture is $V_{EE}\approx3V_{BE}+2V_S$, where V_S is the voltage swing which is taken to be 0.4 V in

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