Origin of the Excess Capacitance at Intimate Schottky Contacts

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We identify the physical origin of the excess capacitance at Schottky diodes without an interfacial layer, i.e., intimate Schottky contacts. Measured capacitance in excess of the space-charge capacitance is shown to be caused by the injection of minority carriers into the bulk semiconductor, rather than by the presence of interface states, as previously thought. Minority-carrier injection depends sensitively on the properties of the Ohmic back-contact.

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The enigma of Schottky barriers at metal/semiconductor contacts still challenges solid-state research. Schottky[1] explained the rectifying properties by a barrier

$$\Sigma = \Phi_m - \chi, \tag{1}$$

where Φ_m is the work function of the metal and χ is the electron affinity of the semiconductor. Deviations from Schottky's model[1] were explained[2] with interface states. The solution of the Schottky-barrier problem was therefore seemingly reducible to interface states.

Significant progress was recently achieved in the theory[3] and in the epitaxial growth[4–6] of Schottky contacts. Understanding of carrier transport was believed to be complete: Schottky contacts are usually treated as pure majority-carrier devices. Minority-carrier injection, a fundamental prerequisite for the bipolar transistor and the birth of solid-state electronics,[7] is usually not discussed in the context of Schottky contacts. However, bipolar transport of electrons *and* holes must also occur in Schottky contacts and, in particular, the diffusing minority carriers should influence the low-frequency capacitance.

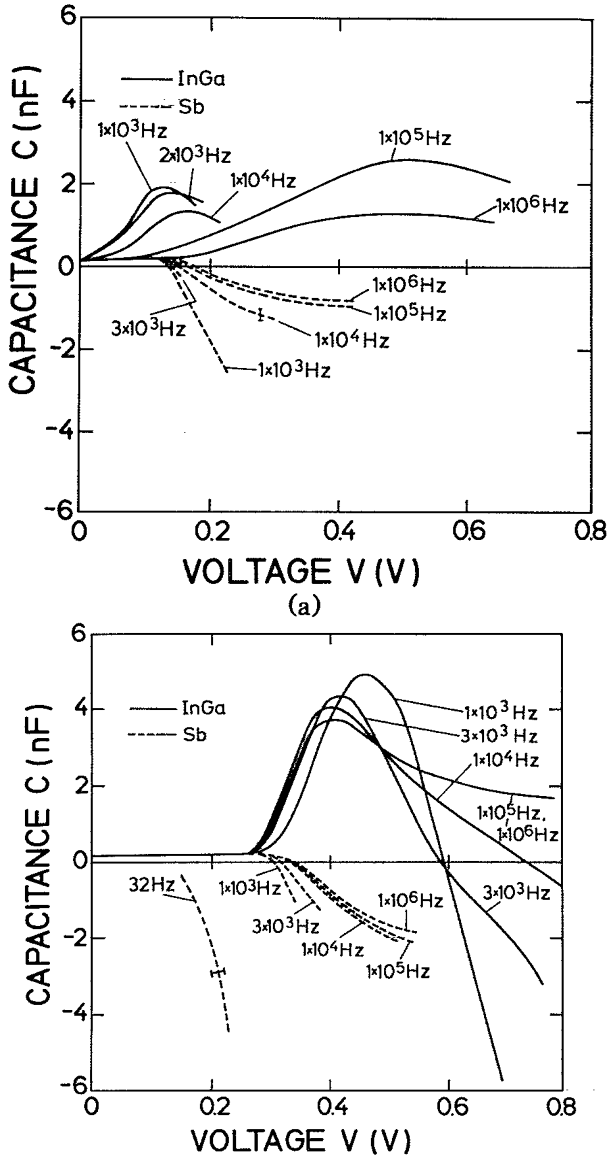
For about fifteen years, low-frequency capacitances in excess of the capacitance C_{sc} of the space-charge region have indeed been observed at forward-biased Schottky diodes. These excess capacitances were, however, not ascribed to minority carriers but to interface states.[8–10] Bardeen's[2] interface states were thought to be measurable with the help of such excess capacitances. The so-called[8] Schottky capacitance spectroscopy and accurate phase capacitance spectroscopy[9,10] are standard characterization methods. We recently[11] demonstrated a fundamental inconsistency in these techniques which violate Gauss's law when applied to Schottky contacts with an interfacial layer. Low-frequency capacitances alone are *not* sufficient to characterize such interfaces.[11] Instead, the complete frequency-dependent admittance has to be analyzed within a self-consistent model such as was used to characterize traps at Au/oxide/GaAs diodes.[11]

Excess low-frequency capacitances at contacts *without* an interfacial layer, i.e., intimate Schottky contacts, were also ascribed to interface states.[8–10] Unfortunately the interpretation is valid for the reasons outlined above. Particularly interesting are epitaxial $NiSi_2$/Si diodes: $NiSi_2$ grows in two distinct orientations (termed types A and B) on silicon (111) surfaces,[4] with a difference of at least 140 meV for the two Schottky barriers.[5] This difference, originally questioned by Liehr *et al.*,[6] was recently challenged: Ho *et al.*[9] measured excess capacitances, interpreted them in terms of interface traps, and claimed to prove *equal* barriers for types A and B due to similar densities and energies of interface states.

The present Letter examines forward-bias low-frequency C/V curves on intimate Schottky contacts. We here furnish the answer to the fundamental question of the real nature of the excess capacitances in the aforementioned[8–10] experiments. In contrast to the current dogma,[9] we find that these spectacular capacitances[8–10] are not caused by interface states but instead by *minority carriers* injected into the bulk semiconductor. This bulk capacitance is in turn controlled by the back-contact. The strong effect of minority carriers and, in particular, the dramatic influence of the *Ohmic* back-contact on admittances of Schottky diodes are here elucidated for the first time.

Our study examines nonepitaxial $NiSi_2$/Si, PtSi/Si, Pd_2Si/Si, as well as epitaxial $NiSi_2$/Si Schottky contacts[4,5] of types A and B with an area of 1×10^{-2} cm^2. Special attention is devoted to the Ohmic back-contacts of our 500-μm-thick wafers. We test implanted P contacts, laser-annealed Sb contacts, Al contacts, and InGa that is mechanically applied to the back side. Sb contacts are fabricated by evaporation and laser annealing of the donor Sb to yield high-quality n^+ contacts.[5] We measure capacitances at 296 K with a Hewlett-Packard model 4192A *LCR* meter and a current source to apply the bias. The precision of our setup is verified with test capacitors and resistors as well as with independent measurements using a lock-in amplifier.

Figures 1(a) and 1(b) show capacitances from two $NiSi_2$ samples of type A and two of type B that are epitaxially[4,5] grown on 4-Ω-cm, *n*-type (111) silicon. The two A-type samples of Fig. 1(a) are — as are the B-type samples of Fig. 1(b) — completely identical apart from their back-contacts. *I*/*V* curves yield $\Sigma=0.63$ eV and an ideality[11] $n=1.02$ for type A, and $\Sigma=0.80$ eV, $n=1.05$ for type B. Our measurements show no capacitance in excess of the capacitance C_{sc} of the space-charge region for Sb contacts. On the contrary, we find inductances. Such inductances are well known from *pn* junctions[12] where they are caused by injected minority carriers that modulate the bulk resistance. The same effect was predicted[13] for Schottky contacts and is here experimentally verified.



(a)

(b)

FIG. 1. (a) Forward-bias *C*/*V* curves for two A-type $NiSi_2/Si$ diodes ($\Sigma=0.63$ eV) at different frequencies. The sample with the Sb back-contact yields no excess capacitance but only an inductance due to conductivity modulation by injected minority carriers. The InGa contact (resistance 17 Ω) yields excess capacitances. (Maximum space-charge capacitance $C_{sc,max}=0.16$ nF.) (b) *C*/*V* curves at a B-type $NiSi_2/Si$ diode ($\Sigma=0.80$ eV) with a Sb back-side contact show no excess capacitance. The InGa contact with 39 Ω contact resistance yields excess capacitances/inductances. ($C_{sc,max}=0.18$ nF.)

The inductances in Figs. 1(a) and 1(b) arise when the voltage drop at the series resistance across the Si substrate is comparable to the voltage at the Schottky barrier. A comparison of the dashed curves in Figs. 1(a) and 1(b) at identical frequencies reveals that the voltages where the capacitances turn negative are higher for the B-type sample. The voltage difference (0.15 V) correlates with the barrier difference because B-type samples with their high barrier require a higher voltage to reach a regime in the *C*/*V* curve where the bulk resistance of the Si (and conductivity modulation) become comparable to the resistance of the Schottky diode.

The curve at 32 Hz in Fig. 1(b) demonstrates that even at very low frequencies there are no excess capacitances. We do not detect any excess capacitance between 5 Hz and 10 MHz that might be ascribable to interface states as long as we use implanted or laser-annealed n^+ contacts. Instead, we always find *inductances* due to minority carriers.

We find excess capacitances only if we deliberately use imperfect back-side contacts with noticeable contact resistances: InGa, Al, or unetched oxides on the back side before evaporation of Sb. The solid curves in Figs. 1(a) and 1(b) show results for InGa contacts: Large capacitance peaks occur. If we correct for the voltage drop across the InGa contact, then the voltage difference between capacitance maxima correlates again roughly with the barrier difference. Ho *et al.*[9] using Al back-contacts, interpreted this correlation as a proof of traps at the Schottky contact on the front side. We repeat their[9] experiments and find also excess capacitances which are, however, traceable to Al and its contact resistance; the acceptor Al is not expected to yield low-resistance contacts to *n*-type Si. Only a precise analysis[14] of *I*/*V* curves yields such contact resistances in addition to the bulk resistance of Si. We find total series resistances (bulk plus contact resistance) of $R_{Sb}=19\ \Omega$ and $R_{InGa}=36\ \Omega$ for the Sb and InGa contacts in Fig. 1(a) as well as $R_{Sb}=13\ \Omega$, $R_{InGa}=52\ \Omega$ for Fig. 1(b).

We ascribe the excess capacitances to minority carriers which are injected by the Schottky contact into the bulk Si and cause there excess *diffusion* capacitances. The first hint of excess injection is the concomitance of the excess capacitance for InGa contacts with an inductance at higher voltages: Conductivity modulation by minority carriers is practically the only inductive effect in semiconductors. Inductances—also observed by the advocates of Schottky capacitance spectroscopy[15] and accurate phase capacitance spectroscopy[16]—are hard to explain with interface states.

Secondly, evidence is supplied by the dependence on the resistance of the back-contact. An interface-state capacitance at the front Schottky diode should not depend on back-contact. Minority carriers explain this dependence: Scharfetter[17] predicted minority-carrier injection in Schottky diodes under dc conditions to depend critically on recombination at the back-contact; the only theoretical treatment of ac conditions[13] unfortunately neglects recombination; no systematic experimental study has been performed. Our data prove back-contact–controlled injection: Injected minority carriers either recombine in the bulk Si or are extracted at the back side. Low-resistance n^+-back-side contacts to n-type Si form a minority-carrier reflecting barrier in the valence band of the nn^+ junction. Injection is therefore suppressed and inductances, as verified in Figs. 1(a) and 1(b) for the Sb contracts, are observable. High-resistance contacts such as Al,[9,10] or InGa suggest, on the other hand, a nn^- junction at the back side with a minority-carrier sink in the valence-band edge. Such extracting contacts support strong injection at the front Schottky diode. Excess diffusion capacitances arise as long as the diffusion length is comparable to sample thickness. Indeed, most excess capacitances were previously measured[8–10] in low-doped silicon with typical diffusion lengths of 100–500 μm.

Thirdly, spatial constancy of the total current j_{tot} requires that the excess capacitive current flows also within the space-charge region of the Schottky diode where the ac voltage $\delta\Phi$ drops. In order to obtain *excess* capacitances, this additional capacitance must be in *parallel* to the space-charge capacitance C_{sc}. Ampère's law for a semiconductor,

$$j_{\mathrm{tot}} = \nabla H = j_n + j_p + \dot{D}, \tag{2}$$

states that the total current j_{tot} consists of the majority-carrier current j_n, the minority-carrier current j_p, and the displacement current $\dot{D}$. There are no other currents which can be made responsible for excess capacitances within any model which is in agreement with Maxwell's electrodynamic equations.

Without an interfacial layer and with an ideality[11] $n \approx 1$ there is no possibility for an out-of-phase modulation of the band bending and therefore no excess capacitance due to a thermionically emitted majority-carrier current j_n.[11] At frequency ω, the displacement current

$$\dot{D} = i\omega C_{\mathrm{sc}} \delta\Phi \tag{3}$$

yields also no excess capacitance; the resistance of the bulk Si makes the band bending change $\delta\Phi$ always *smaller* than the applied ac voltage. The upper Maxwell equation, Eq. (2), leaves therefore only the minority-carrier current j_p for excess capacitances. Indeed, minority carriers in the space-charge region are phase shifted with respect to the band bending change $\delta\Phi$ since their transport through the bulk semiconductor is mainly controlled by diffusion. They can therefore cause a capacitive current

$$j_p^{90} = i\omega C_{\mathrm{diff}} \delta\Phi, \tag{4}$$

with the diffusion capacitance C_{diff} in parallel to the space-charge capacitance C_{sc}.

In addition to these arguments based on the Maxwell equations [Ampère's law, Eq. (2)] our preliminary results[18] obtained from one- and two-dimensional device simulation demonstrate also that the excess capacitance is caused by minority carriers. The calculations, which will be presented in a separate publication,[18] show the capacitances or inductances to depend sensitively on the boundary conditions of the back-contact. Our simulations qualitatively reproduce the observed inductances at $\mathrm{NiSi_2}$ Schottky diodes with a good Ohmic contact. This inductance is influenced by spatial inhomogeneities in the Schottky barrier. The excess capacitance and the observed frequency dependence with a poor Ohmic contact are also reproduced by simulation: We obtain large excess capacitances by including regions of p^+ doping along an inhomogeneous back side as expected when one uses InGa or Al contacts to n-type silicon. In summary,

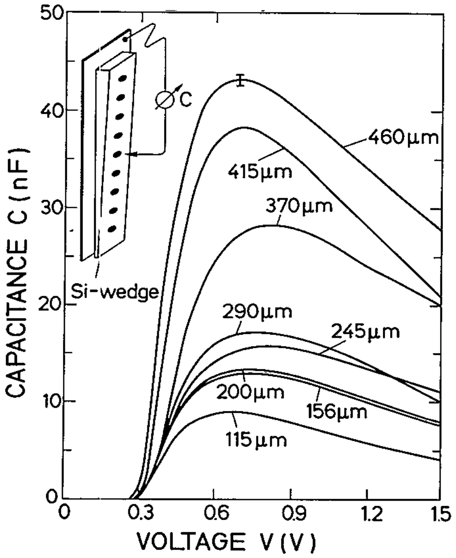


FIG. 2. Different PtSi/Si diodes with $\Sigma = 0.84$ eV on the front of the Si wedge are measured at 1 kHz against the same, single, large-area back-contact. The thickness dependence proves that the excess capacitance originates from the bulk Si and not from the interface of the PtSi/Si diode. ($C_{\mathrm{sc,max}} = 0.08$ nF.)

all the observed capacitance and inductance behavior can be understood by inclusion of minority carriers in the description of the current transport.

An experiment utilizing a wedge as shown in Fig. 2 yields a striking *experimental* proof that the excess capacitance truly originates in the bulk Si: We evaporate Pt dots (area 5.6×10^{-3} cm^2) onto a 11-Ω-cm, *n*-type silicon wedge and form PtSi/Si diodes with Σ=0.84 eV, n=1.07 by heating at 400 °C. The wedge has a single, large-area, evaporated and laser-annealed Sb back-contact. The I/V curves of all Schottky contacts yield a series resistance around 250 Ω. This value is almost totally due to the contact resistance of the common back-side contact being of high resistance because we did not etch the native SiO$_2$ before evaporating the Sb. The thickness dependence of the maxima in Fig. 2 is due to the different volume of stored minority carriers and demonstrates that the excess capacitance is a bulk property. The Schottky diodes inject minority carriers and the back-side contact extracts them. Excess diffusion capacitance and inductive conductivity modulation add to give C/V maxima.

We conclude the following:

(i) Intimate Schottky contacts (without interfacial layers) with low-resistance, Ohmic, minority-carrier–reflecting n^+-back-side contacts show only inductive conductivity modulation. We find no excess interface-state capacitance.

(ii) Imperfect back-contacts cause the excess[8-10] capacitances. We ascribe this effect to diffusing minority carriers. Minority-carrier *extracting* back-contacts facilitate *injection* at the front Schottky diode. Minority carriers flow out of phase with the applied voltage since their transport through the bulk is controlled by diffusion.

(iii) Previously reported excess capacitances[8-10] at intimate Schottky contacts were probably caused not by interface states but by imperfect back-contacts and minority-carrier injection. Therefore, such measurements[9] constitute no proof for similar interface states at NiSi$_2$/Si diodes[4-6] of types A and B but are rather a sensitive tool for the characterization of *back-side* contacts.

(iv) Care should be taken to ensure that excess capacitance ascribed to interface states at intimate Schottky contacts with idealities $n\approx1$ are not, in fact, caused by minority carriers. In addition, any such interpretation should be shown to be consistent with Maxwell's equations [e.g., Ampère's law, Eq.(2)].

(v) The measurability of interface states at Schottky contacts requires an interfacial layer, which separates the traps from the metal and allows for an out-of-phase modulation of the semiconductor's band bending due to trapping. The traps are then detectable via capacitive majority-carrier currents j_n and displacement currents $\dot{D}$ in the interfacial layer.[11] I/V curves and frequency-dependent admittances as well as a model[11] obeying Gauss's and Ampère's law are, however, a minimum requirement for a self-consistent analysis.

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