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Graphene-Silicon Schottky Diodes

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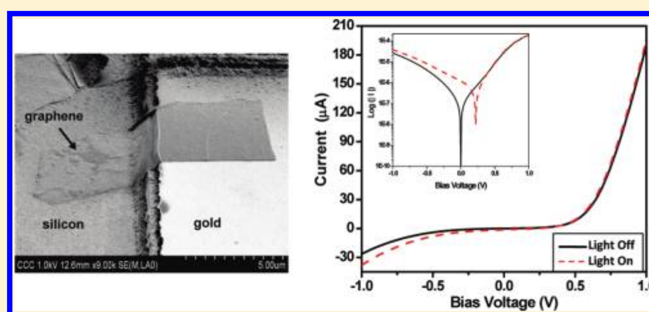
Supporting Information

ABSTRACT: We have fabricated graphene-silicon Schottky diodes by depositing mechanically exfoliated graphene on top of silicon substrates. The resulting current−voltage characteristics exhibit rectifying diode behavior with a barrier energy of 0.41 eV on *n*-type silicon and 0.45 eV on *p*-type silicon at the room temperature. The $I-V$ characteristics measured at 100, 300, and 400 K indicate that temperature strongly influences the ideality factor of graphene−silicon Schottky diodes. The ideality factor, however, does not depend strongly on the number of graphene layers. The optical transparency of the thin graphene layer allows the underlying silicon substrate to absorb incident laser light and generate a photocurrent. Spatially resolved photocurrent measurements reveal the importance of inhomogeneity and series resistance in the devices.



KEYWORDS: Graphene, silicon, Schottky, diode, photocurrent

Extensive transport studies have been performed on individual-, double- and few-layer graphene,[1−8] since it was first exfoliated from graphite onto dielectric substrates in 2004.[9] Researchers have made p-n junctions by electrostatically gating single layer graphene (SLG).[10−12] Because of its high electron mobility (200,000 cm^2/V s), and high electric current carrying capacity (>10^8 A/cm^2), graphene is an excellent candidate for next-generation field effect transistors.[13−17] Graphene has the advantages over carbon nanotubes of being naturally compatible with thin film processing, enabling large device areas and, hence, high operating powers. Also, graphene is more readily scalable and has lower contact resistance. Nagashio et al. have successfully evaluated the contact resistance between graphene and several most common electrodes, including Ti/Au, Cr/Au, and Ni, which are patterned and deposited on graphene using electron-beam lithography and electron gun evaporation. Through four probe measurements, the lowest contact resistance ∼500 $\Omega\mu$m was observed from the interface of graphene and Ni.[18,19]

Schottky barriers of energy ∼0.7 eV have been observed in graphene/graphene-oxide junctions and can be easily tuned by changing the oxidation temperature.[20] Schottky barriers made from graphene nanoribbons have been simulated theoretically. In simulations performed by Jiménez et al., the Schottky barrier depletion width reduces and the tunneling current increases as the gate voltage increases.[21,22] Epitaxially grown graphene/graphene-oxide junctions have also demonstrated Schottky diode behavior, as a consequence of the band gap in graphene oxide.[23] While many previous studies have explored electron transport in graphene, the Schottky barriers between graphene and silicon have not been studied thoroughly. Tongay et al. have observed the Schottky barriers at bulk HOPG graphite−silicon interfaces.[24] Here, no photocurrents could be measured, and a comparison of n- and p-type substrates was not given in this prior work. Also, the local effect of light absorption on the $I-V$ characteristics of graphene/silicon interfaces has not been studied. We present a detailed study of the graphene−silicon interface, including temperature dependence, graphene layer thickness dependence, and spatial mapping of photocurrents, which will likely be important for the future integration of graphene with silicon.

We fabricate graphene−silicon Schottky diodes by depositing graphene on top of the $Si/SiO_2/Si_3N_4/Cr/Au$ structure shown in Figure 1a. To obtain a clean Si−graphene interface, the SiO_2 is removed by BOE 7:1 wet etching. The samples are then rinsed with DI water and baked on a hot plate at 120 °C to remove any water from the surface. After wet etching, we perform dry etching using CF_4 RIE.[25] These processing steps remove the native oxide on the Si and passivate the surface.[26] Graphene is then deposited by mechanical exfoliation in air. All samples were fabricated under the exact same conditions. While we have no way of knowing the precise atomic configuration at the Si−graphene interface, the dry etching step is crucial in order to fabricate devices with finite resistance exhibiting rectifying $I-V$ characteristics. According to Bunch et al., graphene flakes are gas impermeable,[27] which ensures that no further oxidation of the Si surface occurs at the Si−graphene interface through the graphene flakes once they are deposited. In addition, Chen et al. also demonstrated that graphene, grown by chemical vapor deposition on copper, is able to prevent the underlying copper surface from air oxidation,[28] further corroborating that no oxidation is taking place after the graphene deposition. Since

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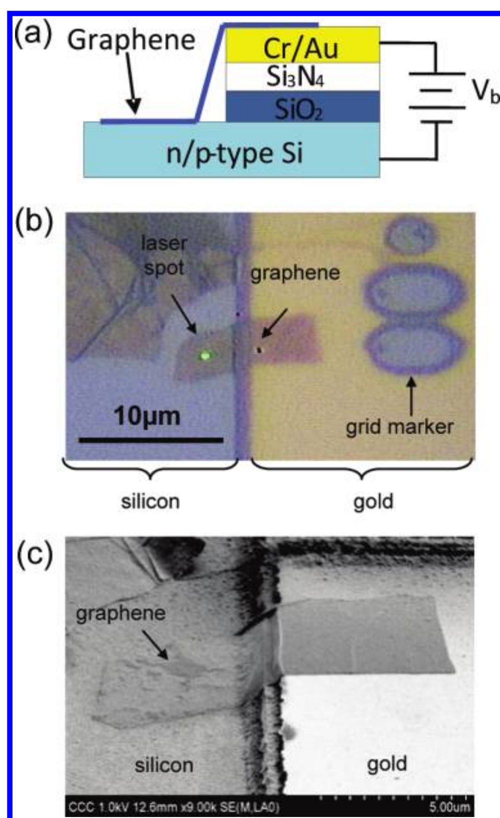

Figure 1. (a) Schematic diagram, (b) optical micrograph, and (c) SEM image of a graphene on n-type silicon Schottky diode.

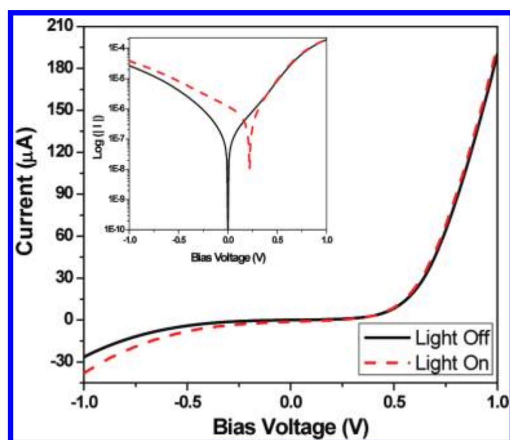

Figure 2. Current−voltage characteristics of a graphene on n-Si device with and without illumination. The inset figure shows current on a log scale.

the native oxide on silicon surfaces is usually less than 10 Å thick,[29] the native oxide should only affect a very small region near the outer edge of the graphene device. We have evaluated the stability and time dependence of these devices by comparing the $I-V$ characteristics taken immediately following device fabrication with those taken after one week in an ambient environment. This data is presented in the Supporting Information, which shows no change or degradation in $I-V$ behavior, and therefore no increased oxide or tunnel barrier. To characterize the device, a bias voltage (V_b) is applied between the Au electrode and Si substrate, as shown in Figure 1a. All measurements were taken at room temperature and ambient conditions, unless otherwise stated. A graphene bilayer deposited on an n-type Si substrate ($n \sim 2.5 \times 10^{15}$ cm^{-3}) with a Au electrode can be seen in the optical microscope and scanning electron microscope (SEM) images shown in Figure 1b,c. Figure 1b shows illumination from an approximately 0.5 μm diameter 532 nm wavelength laser spot.

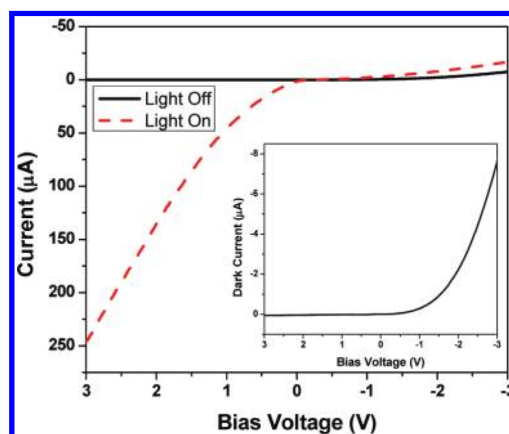

Figure 3. Current−voltage characteristics of a graphene on p-Si Schottky diode with and without illumination. Inset shows the enlarged dark current−voltage characteristics.

Figure 2 is the measured $I-V_{bias}$ characteristics of the graphene−silicon device shown in Figure 1 taken with and without illumination. Here, the Au makes an Ohmic contact to the graphene, while the silicon-graphene interface forms a Schottky barrier, which exhibits rectifying behavior. The contact resistances between Au and graphene are estimated from four-probe measurements to be approximately 212 × 10^{-6} Ω cm^2.[18,19] On the basis of this result, the contact resistances between silicon and graphene are estimated to be ∼73.6 × 10^{-6} Ω cm^2 from the linear region of the $I-V_{bias}$ characteristics (from 0.6 to 1.0 V), as shown in Figure 2. The lower contact resistance indicates the bonding energy of graphene−silicon interface (151 ± 28 mJ/m^2) is slightly higher than that of graphene−Au interface (∼160 mJ/m^2).[30,31] In these experiments, approximately 30 mW of laser power uniformly illuminate the graphene flake. The finite photocurrent and open circuit voltage can be seen more clearly in the inset, indicating photoexcitation of carriers and photocurrent generation.

Graphene bilayers deposited on the p-type Si substrates ($p \sim 1.25 \times 10^{14}$ cm^{-3}) were also studied. As shown in Figure 3, the $I-V_{bias}$ data of this device taken with and without uniform laser illumination exhibits rectifying behavior under negative applied voltages. In the inset of Figure 3, the rectifying $I-V_{bias}$ curve taken without illumination is enlarged, demonstrating the Schottky barrier formed between graphene and p-Si. In this device, a 250 μA photocurrent is observed at V_{bias} = 3 V under 532 nm laser illumination.

Spatially mapped photocurrents were also measured on the graphene-silicon device shown in Figure 1. Figure 4a shows an optical image of the device, together with the grid used to measure the photocurrents shown in Figure 4b. Here, a 10 mW laser beam is focused to a 0.5 μm spot size and irradiated at every intersection of the grid, separately, while $I-V$ data is taken. The photocurrent map presented in Figure 4b plots the current distribution over the device area at V_b = 0 V. The current map shows very weak photocurrent generation in regions without graphene, and the current tends to be higher in the region closer

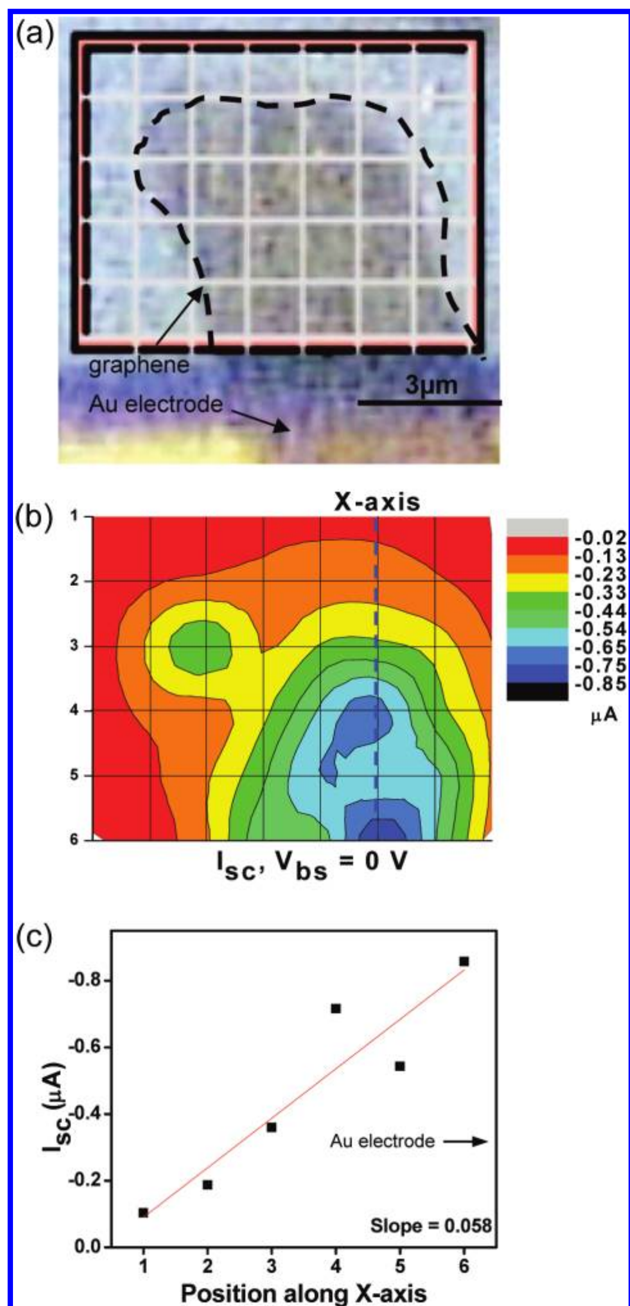

Figure 4. (a) Optical microscope image of a graphene flake and gold electrode. (b) Short-circuit photocurrent spatial map. (c) Short-circuit photocurrent along the *X*-axis of the short-circuit photocurrent map in (b).

to the Au electrodes. A plot of the spatial dependence of the short circuit photocurrent (Figure 4c) exhibits a linear spatial dependence, which is consistent with the series resistance hypothesis put forth in this paper. Here, the in-plane resistance creates an effective load resistance in the circuit, which causes the measured photocurrent to be reduced when illuminating away from the gold electrode under the same laser intensity. An alternative explanation of the spatial dependence of the photocurrent is oxidation driven by oxygen diffusion from the graphene−silicon edge. However, if it were due to oxidation, any spatial variation in photocurrent due to the oxide thickness would result in large changes spanning orders of magnitude, rather than the ∼4× changes observed in our measurements.

The current−voltage characteristics of the graphene on n-type and p-type silicon devices were also measured at temperatures T = 100, 300, and 400 K without illumination, as shown in Figure 5. Here, the current increases as the temperature increases in both n-type and p-type devices, due to thermally excited electrons, which enhance the carrier concentration in the underlying silicon substrates.[32,33] The current measured at T = 400 K is over 400 times that observed at T = 100 K in p-Si devices at $V_b = -3$ V, as shown more clearly in the inset of Figure 5b.

The current flowing across a Schottky diode can be expressed by the ideal diode equation

$$I = I_o\left(\frac{eV_{bias}}{e^{n_{id}k_BT} - 1}\right) \quad (1)$$

where I_o is the reverse saturation current and n_{id} is the ideality factor. For an ideal diode, n_{id} = 1, and n_{id} > 1 for nonideal diodes.[34] A fit of the data shown in Figure 2 yields an ideality factor of 4.89. The ideality factors of several devices are listed in Table 1, and range from 4.89 to 7.69 for n-Si devices and 29.67 to 33.50 for p-Si devices at room temperature. The largest ideality factor among the n-Si diodes, 7.69, corresponds to a three layer graphene-silicon diode, however, no obvious dependence of the ideality factor on graphene layers was observed.

Figures 2 and 3 illustrate three major differences between n-Si and p-Si substrate graphene Schottky diodes, including turn-on bias, current intensity, and photocurrent. First, the n-Si device is turned on with a positive bias and p-Si device with a negative bias, due to the different majority carriers in the substrate. Second, the magnitude of the current density in the n-Si devices is significantly higher than those measured in the p-Si devices. For instance, the current density of sample N7P2 is 8.24×10^6 A/m^2 at V_b = 1 V, while that of sample P1P3 is only 4.59×10^5 A/m^2 at $V_b = -3$ V. The saturation current, I_o, in eq 1 can be expressed as

$$I_o = A^*T^2e^{-\frac{e\varphi_{Bn/p}}{k_BT}}A \quad (2)$$

and

$$\varphi_{Bn/p} = \frac{k_BT}{e}\ln\left[\frac{AA^*T^2}{I_o}\right] \quad (3)$$

where A is the graphene−Si contact area, A^* is the effective Richardson's constant, which is 112 A cm^{-2} K^{-2} for n-Si and 32 A cm^{-2} K^{-2} for p-Si substrates,[35] and $\varphi_{Bn/p}$ is the Schottky barrier. From eqs 2 and 3, the Schottky barriers are estimated to be 0.41 eV on average for the bilayer graphene n-Si devices and 0.44 eV for the bilayer graphene p-Si device at 300 K, which is consistent with the higher current densities observed in n-Si devices versus p-Si devices. These values are considerably smaller than the Schottky barrier heights (∼0.7 eV) measured previously in graphene/graphene-oxide interfaces.[20] The third difference between n-Si and p-Si devices is the photocurrent. Unlike the dark current, the photocurrent is more pronounced in p-Si devices (under positive bias) than in n-Si devices (under negative bias). The photocurrent in p-Si devices is 45.8 μA (under V_{bias} = 1 V and 30 mW uniform laser illumination), while it is only 11.7 μA in n-Si devices (under $V_{bias} = -1$ V and 30 mW uniform laser illumination). The steady-state photocurrent density of Schottky diode is expressed as

$$J_L = eWG_L \quad (4)$$

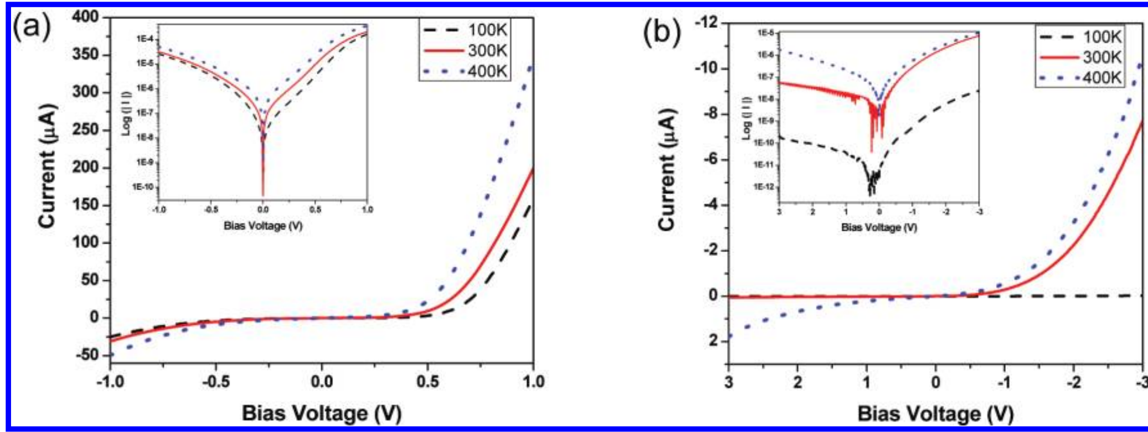

Figure 5. Current−voltage characteristics measured at T = 100, 300, and 400 K for (a) an n-Si device and (b) a p-Si device. The inset figures show current on a log scale.

Table 1. Summary of Data Taken on Several Different Graphene−Silicon Schottky Diode Devices

				ideality factor			$\varphi_{Bn/p}$ (eV)		
sample	number of graphene layers	graphene−Si contact area (μm^2)	substrates	100 K	300 K	400 K	100 K	300 K	400 K
N7P1	2	64.2	n-Si	12.6	5.39	6.67	0.128	0.415	0.495
N7P2	2	24.2	n-Si	11.8	4.89	4.25	0.127	0.416	0.403
N7P3	2	19.0	n-Si	13.4	5.80	5.82	0.118	0.406	0.480
N5P1	3	92.0	n-Si	16.6	7.69	na	0.128	0.425	na
P1P3	2	16.9	p-Si	89.0	29.7	27.6	0.131	0.436	0.491
P1P1	multiple	57.9	p-Si	82.6	33.5	24.9	0.144	0.46	0.558

where G_L is the generation rate of excess carriers, W is the space charge region width, and is expressed as

$$W = \left[\frac{2\epsilon_s(V_{bi} + V_R)}{eN_{d/a}}\right]^{1/2} \quad (5)$$

$$V_{bi} = \varphi_{Bn/p} - \varphi_{n/p} \quad (6)$$

where

$$\varphi_{n/p} = E_{c/v} - E_{Fi} = KT \ln\left(\frac{N_{c/v}}{N_{d/a}}\right) \quad (7)$$

and N_d ($\sim 2.5 \times 10^{15}$ cm^{-3}) and N_a ($\sim 1.25 \times 10^{14}$ cm^{-3}) are the carrier concentrations, ϵ_s is permittivity of silicon, V_R is the applied reverse-bias voltage, and N_c ($\sim 2.8 \times 10^{19}$ cm^{-3}) and N_v ($\sim 1.09 \times 10^{19}$ cm^{-3}) are the effective density of states functions in the conduction and valence bands.[36] Taking, for example, samples N7P2 and P1P3 at $V_R = -1$ V and 300 K, eqs 5, 6, and 7 give φ_n = 0.242 eV, φ_p = 0.295 eV, and W(N7P2) = 9.51 × 10^{-5} cm, W(P1P3) = 3.82 × 10^{-4} cm. The contact area of sample N7P2 is 24.2 μm^2 and 16.9 μm^2 for sample P1P3; these result in the photocurrent ratio (I_{N7P2}/I_{P1P3}) to be 0.356, which is slightly higher than the experimental value (0.255). However, the differences of space charge region width here are still believed to be the major factor for the higher photocurrents observed in p-Si devices. Equation 3 indicates that the ambient temperature has a major influence on the Schottky barriers. This can be seen in Table 1, which shows how Schottky barrier heights vary with temperature. Unlike the $I-V$ characteristic shown in Figure 5, Table 1 indicates that the Schottky barriers decrease as the temperature decreases, while Figure 5 shows the current increases at high temperature. These results imply that the current intensity is dominated by thermal excitation instead of Schottky barriers height.

Figure 6 shows the $I-V$ characteristics of a p-Si diode measured in air at 300 K before and after the device was annealed in vacuum at 200 °C for 20 h. The Raman spectra exhibit G band upshifts of 4.6 cm^{-1} and linewidth narrowing of 2.8 cm^{-1} after the vacuum annealing. According to Remero et al., graphene FET devices exposed in air for several days are found to be p-type and after kept in vacuum for 20 h at 200 °C, the devices became n-type.[37] Therefore, the variations in the Raman spectra and $I-V$ characteristics in vacuum shown in Figure 6 are believed to be due to the n-type doping of the graphene in vacuum.[38] This n-type doping results in the observed G band upshift and line width narrowing, and causes a 0.036 eV increase in the Schottky barrier. This observation implies that the Schottky barrier between graphene and the underlying silicon substrate can be modified by individually doping the graphene.

Strain in the intermediate region between the Si and gold contact regions could also affect the device transport characteristics. We have ruled out the possibility of strain in this intermediate region by measuring the Raman spectra, which show G band modes in the range of 1582 to 1585 cm^{-1}, which is similar to normal unstrained graphene.[39,40] Any appreciable strain would result in a significant downshift of this vibrational mode (14.2 cm^{-1}/% for single layer and 12.1 cm^{-1}/% for three layer graphene), as observed by Ni et al. and Yu et al.[41,42]

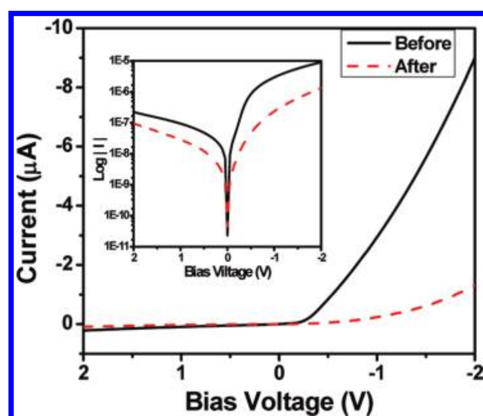

Figure 6. Current−voltage characteristics of a graphene on p-Si Schottky diode before and after vacuum annealing.

In conclusion, the $I-V$ characteristics of graphene−silicon interfaces indicate that a Schottky barrier is formed at the interface between the graphene and silicon. The magnitude of the photocurrent flowing across the graphene−silicon devices is spatially dependent, possibly due to the in-plane series resistance of the graphene. The electrical current of these devices is also affected by the temperature. Devices at higher temperatures tend to conduct more strongly. Lastly, both current intensity and ideality factor do not show obvious dependence on the graphene thickness.

ASSOCIATED CONTENT

Supporting Information. Additional figure. This material is available free of charge via the Internet at http://pubs.acs.org.

ACKNOWLEDGMENT

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REFERENCES

(1) Stauber, T.; Peres, N. M. R.; Guinea, F. *Phys. Rev. B* **2007**, *76* (20), 205423.

(2) Katsnelson, M. I.; Geim, A. K. *Philos. Trans. R. Soc. London, Ser. A* **2008**, *366* (1863), 195–204.

(3) Cresti, A.; Nemec, N.; Biel, B.; Niebler, G.; Triozon, F.; Cuniberti, G.; Roche, S. *Nano Res.* **2008**, *1* (5), 361–394.

(4) Laakso, M. A.; Heikkila, T. T. *Phys. Rev. B* **2008**, *78* (20), 205420.

(5) Ouyang, F. P.; Wang, H. Y.; Li, M. J.; Xiao, J.; Xu, H. *Acta Phys. Sin.* **2008**, *57* (11), 7132–7138.

(6) Das Sarma, S.; A., S.; Hwang, E. H.; Enrico Rossi *Rev. Mod. Phys.* **2010**submitted for publication.

(7) Geim, A. K. *Science* **2009**, *324* (5934), 1530–1534.

(8) Castro Neto, A. H.; G., F.; Peres, N. M. R.; Novoselov, K. S.; Geim, A. K. *Rev. Mod. Phys.* **2009**, *81* (1), 109–162.

(9) Novoselov, K. S.; Geim, A. K.; Morozov, S. V.; Jiang, D.; Zhang, Y.; Dubonos, S. V.; Grigorieva, I. V.; Firsov, A. A. *Science* **2004**, *306* (5696), 666–669.

(10) Liu, G.; Velasco, J.; Bao, W. Z.; Lau, C. N. *Appl. Phys. Lett.* **2008**, *92* (20), 203103.

(11) Williams, J. R.; DiCarlo, L.; Marcus, C. M. *Science* **2007**, *317* (5838), 638–641.

(12) Williams, J. R.; Abanin, D. A.; DiCarlo, L.; Levitov, L. S.; Marcus, C. M. *Phys. Rev. B* **2009**, *80* (4), 045408.

(13) Wu, J. Y.; Chiu, Y. H.; Lien, J. Y.; Lin, M. F. *J. Nanosci. Nanotechnol.* **2009**, *9* (5), 3193–3200.

(14) Xia, F. N.; Farmer, D. B.; Lin, Y. M.; Avouris, P. *Nano Lett.* **2010**, *10* (2), 715–718.

(15) Lin, Y. M.; Dimitrakopoulos, C.; Jenkins, K. A.; Farmer, D. B.; Chiu, H. Y.; Grill, A.; Avouris, P. *Science* **2010**, *327* (5966), 662–662.

(16) Lin, Y. M.; Chiu, H. Y.; Jenkins, K. A.; Farmer, D. B.; Avouris, P.; Valdes-Garcia, A. *IEEE Electron Device Lett.* **2010**, *31* (1), 68–70.

(17) Bolotin, K. I.; Sikes, K. J.; Jiang, Z.; Klima, M.; Fudenberg, G.; Hone, J.; Kim, P.; Stormer, H. L. *Solid State Commun.* **2008**, *146* (9−10), 351–355.

(18) Nagashio, K.; Nishimura, T.; Kita, K.; Toriumi, A. *2009 IEEE Int. Electron Devices Meet.* **2009**, 527–530.

(19) Russo, S.; Craciun, M. F.; Yamamoto, M.; Morpurgo, A. F.; Tarucha, S. *Physica E* **2010**, *42* (4), 677–679.

(20) Wu, X. S.; Sprinkle, M.; Li, X. B.; Ming, F.; Berger, C.; de Heer, W. A. *Phys. Rev. Lett.* **2008**, *101* (2), 026801.

(21) Yoon, Y.; Fiori, G.; Hong, S.; Iannaccone, G.; Guo, J. *IEEE Trans. Electron Devices* **2008**, *55* (9), 2314–2323.

(22) Jimenez, D. *Nanotechnology* **2008**, *19* (34), 345204.

(23) Alam, K. *Semicond. Sci. Technol.* **2009**, *24* (1), 015007.

(24) Tongay, S.; Schumann, T.; Hebard, A. F. *Appl. Phys. Lett.* **2009**, *95* (22), 222103–222105.

(25) Kastenmeier, B. E. E.; Matsuo, P. J.; Beulens, J. J.; Oehrlein, G. S. *J. Vac. Sci. Technol., A* **1996**, *14* (5), 2802–2813.

(26) Lee, H. Y.; Kim, D. W.; Sung, Y. J.; Yeom, G. Y. *Jpn. J. Appl. Phys., Part 1* **2005**, *44* (3), 1445–1449.

(27) Bunch, J. S.; Verbridge, S. S.; Alden, J. S.; van der Zande, A. M.; Parpia, J. M.; Craighead, H. G.; McEuen, P. L. *Nano Lett.* **2008**, *8* (8), 2458–2462.

(28) Chen, S. S.; Brown, L.; Levendorf, M.; Cai, W. W.; Ju, S. Y.; Edgeworth, J.; Li, X. S.; Magnuson, C. W.; Velamakanni, A.; Piner, R. D.; Kang, J. Y.; Park, J.; Ruoff, R. S. *ACS Nano* **2011**, *5* (2), 1321–1327.

(29) Morita, M.; Ohmi, T.; Hasegawa, E.; Kawakami, M.; Ohwada, M. *J. Appl. Phys.* **1990**, *68* (3), 1272–1281.

(30) Zong, Z.; Chen, C. L.; Dokmeci, M. R.; Wan, K. T. *J. Appl. Phys.* **2010**, *107* (2), 026104.

(31) Vanin, M.; Mortensen, J. J.; Kelkkanen, A. K.; Garcia-Lastra, J. M.; Thygesen, K. S.; Jacobsen, K. W. *Phys. Rev. B* **2010**, *81* (8), 081408.

(32) Xiao, Z. X.; Wei, T. L. *Solid-State Electron.* **1995**, *38* (10), 1837–1838.

(33) Morin, F. J.; Maita, J. P. *Phys. Rev.* **1954**, *96* (1), 28–35.

(34) Levi, A. F. J. *Applied Quantum Mechanics*, 2nd ed.; Cambridge University Press: New York, 2006.

(35) Tung, R. T.; Ng, K. K.; Gibson, J. M.; Levi, A. F. J. *Phys. Rev. B* **1986**, *33* (10), 7077–7090.

(36) Neamen, D. A. *Semiconductor Physics And Devices*, 3rd Ed.; McGraw-Hill: New York, 2003.

(37) Romero, H. E.; Shen, N.; Joshi, P.; Gutierrez, H. R.; Tadigadapa, S. A.; Sofo, J. O.; Eklund, P. C. *ACS Nano* **2008**, *2* (10), 2037–2044.

(38) Yan, J.; Zhang, Y. B.; Kim, P.; Pinczuk, A. *Phys. Rev. Lett.* **2007**, *98* (16), 166802.

(39) Ferrari, A. C.; Meyer, J. C.; Scardaci, V.; Casiraghi, C.; Lazzeri, M.; Mauri, F.; Piscanec, S.; Jiang, D.; Novoselov, K. S.; Roth, S.; Geim, A. K. *Phys. Rev. Lett.* **2006**, *97* (18), 187401.

(40) Ni, Z. H.; Wang, Y. Y.; Yu, T.; Shen, Z. X. *Nano Res.* **2008**, *1* (4), 273–291.

(41) Ni, Z. H.; Yu, T.; Lu, Y. H.; Wang, Y. Y.; Feng, Y. P.; Shen, Z. X. *ACS Nano* **2008**, *2* (11), 2301–2305.

(42) Yu, T.; Ni, Z. H.; Du, C. L.; You, Y. M.; Wang, Y. Y.; Shen, Z. X. *J. Phys. Chem. C* **2008**, *112* (33), 12602–12605.