INVITED PAPER

Towards Quantum Engineering

It may be possible to configure atoms, molecules and nanoscale structures to provide desirable physical properties for future electronic device designs.

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ABSTRACT | Control of material composition at the nanometer and atomic scale dramatically increases electronic device design space due, in part, to quantum effects. New engineering tools are needed to explore this space and ensure that the best, technologically significant device designs are discovered in a most efficient manner. Using a few prototype examples, this paper describes how a methodology for synthesis might be implemented to advance quantum engineering for electronics.

KEYWORDS | Adaptive quantum design; bipolar transistors; device synthesis; high-speed electronics; optimal control; optimal design; optimization; quantum effect semiconductor devices; quantum engineering; quantum systems; transistors

I. INTRODUCTION

Remarkably, reductions in the size of transistors and related technology[1] have allowed "Moore's law" [1], [2] to be sustained for more than 35 years (see Fig. 1). However, the impossibility of continued reduction in transistor device dimensions may be illustrated by an extrapolated dynamic random access memory (DRAM) cell size less than that of an atom by the year 2030. Well before this end-point is reached, quantum effects will dominate device performance, and conventional electronic circuits will fail to function.

As systems transition to a post–Moore's law era, the approach to system innovation will change and the probability of unanticipated technological advances will increase. In part for this reason, large companies such as IBM work hard to track and document trends in electronic device technology [3], [4]. Increased chip complexity also places stress on other parts of the system such as packaging [5] and input/output (IO) interconnects [6], and the consequences can be unexpected. For example, complementary metal–oxide–semiconductor (CMOS) with a 10 nm minimum feature size enables 100 000 000 general-purpose logic transistors and nine high-speed IOs per square millimeter. Individual transistors with cutoff frequency $f_T = 400$ GHz allows an 80 Gb/s off-chip data transfer rate per differential IO pair using PAM-4 [7] coding. This 40 Gbaud/s signaling could operate with point-to-point backplane interconnects over lengths of up to 0.5 m in low-loss media with each link consuming 400 mW of power. The power dissipated per square millimeter chip using such narrow-fast IO might require advanced thermal management strategies such as spray cooling. An alternative approach consisting of electrical IO operating at 10 Gb/s increases packaging complexity due to the increased number

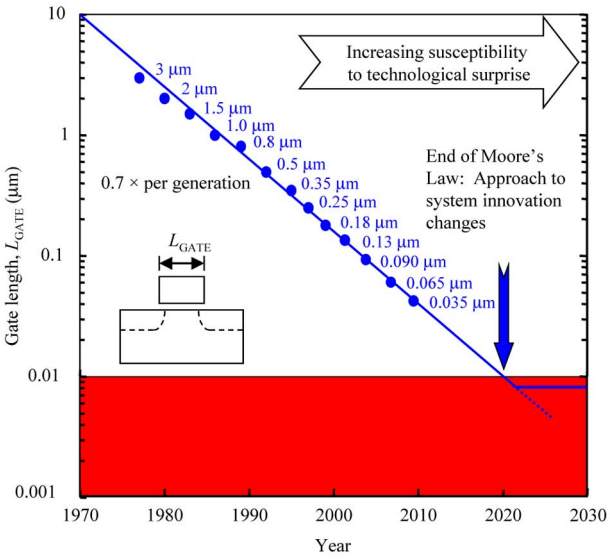

Fig. 1. *Diagram illustrating reduction in CMOS gate length with time. Gate length has been decreasing, or scaling, consistently for the past 35 years. However, physical and other limitations to continued scaling will impact by about the year 2020, and Moore's law will come to an end. As this end-point nears, fundamental changes in the approach to system innovation are required, and there is an increasing susceptibility to technological surprise.*

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[1]http://www.sematech.org.

of signal lines required to achieve the same bandwidth. Such IO may be characterized as slow-wide and is suited for direct interface to existing parallel optical interconnects [8]. Slow-wide IO also has the advantage of simplified radio-frequency design compared to narrow-fast IO.

This example of a potential *divergence* in technical approach for chip and subsystem IO is indicative of the increased possibility of *technological surprise* during the transition period at the end of the Moore's law era. Technological surprise, with enormous value to the owner of the technology, can occur anywhere in the system. Unfortunately, the use of sophisticated numerical optimal design techniques to resolve issues such as subsystem IO is not easily implemented due of the enormous complexity of systems. However, because of its core function, relative simplicity, and susceptibility to innovation, a better starting point is the design of actual devices such as transistors. It is, for example, unknown how practical transistor device design can transition into the quantum regime. In part for these reasons, it seems sensible to explore aspects of current understanding with a view to reexamining the approach to device design.

II. CHALLENGES FOR SCALED TRANSISTORS

Much has been discussed and studied about the continued reduction in size of silicon-based field-effect transistors (FETs) that form the basis of today's CMOS electronics. While there are many significant engineering challenges to be overcome, there seems to be a consensus that a manufacturable technology with minimum feature sizes below 10 nm is achievable [4]. This confidence is based partly on improvements in lithography tools and partly on experience overcoming previously declared limits to scaling [9]. However, just how these designs are to be achieved and what materials and physical effects will be exploited is unresolved. The design methodology seems to be dominated by ad-hoc incremental improvement over what has gone before. Such an approach is, itself, increasingly susceptible to the unexpected.

For example, as one reduces gate length and minimum feature size of a Si FET, one must also reduce the SiO_2 gate-oxide thickness to maintain device performance. This is because in simple models, transconductance is proportional to gate capacitance. For very small minimum feature sizes, the transistor can no longer function since oxide thickness is so small that electrons efficiently tunnel from the metal gate into the source drain channel [10]. The naïve scaling of FETs with a 25-nm gate length requires the physical SiO_2 gate-oxide thickness be reduced on average to 0.7 nm. Such a gate oxide is only four Si atoms thick and because there are two interfaces—one for the metal gate and one for the channel—that are not completely oxidized, the oxide may be thought of as two Si atomic layers thick. This leaves a physically thin tunnel barrier for electrons and contributes to an undesirable tunnel current. Small variations in oxide thickness over a significant area under the transistor gate can further increase leakage current due to electron tunneling between the metal gate and the source-drain channel.

The fact that SiO_2 is made up of discrete atoms is a *structural limit*. So, in addition to electron tunneling, there are structural limits to the scaling of conventional FETs [11], [12].

To avoid some of these difficulties, there is a desire to develop a gate insulator that would allow a thicker dielectric insulator layer to be used in transistor fabrication. For a constant gate capacitance, the way to achieve this is to increase the dielectric's relative permittivity ε_r. Unfortunately, using known material properties, there are limits to how far this approach may be exploited. Nevertheless, there is interest in establishing a so-called high-k (corresponding to high value of ε_r) dielectric technology [13] because if new materials can be found, it would have a significant impact on the scaling of conventional devices.

Another area where the discrete nature of atoms plays a critical role in scaled FETs is the use of substitutional impurities to control carrier concentrations. Random distributions of such impurities in the source, drain, and channel can result in undesirably large variations in transistor turn-on threshold voltage. In fact, because the maximum attainable bulk n-type doping levels in Si of near 3×10^{20} cm^{-3} corresponds to an average impurity spacing of 1.5 nm, any structure just a few times this scale will be strongly influenced by the exact configuration of dopant atoms. This is, of course, an undesirable effect. However, it is conceivable that advanced materials processing and atomic layer control of dopant atoms can be used to create an ordered array of impurities. In this case, the probability of electrons scattering off ionized impurities could be minimized [14], thereby improving electron mobility and reducing channel access resistance. In addition, such materials would significantly reduce this cause of transistor threshold variations.

Surprisingly, there is some experimental evidence that ordered arrays of electrically active dopant atoms can be achieved in Si [15], [16]. Exploration of these effects is only possible because of the existence of controlled monolayer-by-monolayer single-crystal Si growth using molecular beam epitaxy (MBE). If dopant atoms with highly correlated spatial order could be reliably manufactured, the consequences for device design would be dramatic.

Another example of potential for the unexpected in transistor design is extreme nonequilibrium or "ballistic" electron transport. The effect, which many have concluded is detrimental to transistor performance [17], [18], can dominate electron transport in nanoscale devices. Unfortunately, extreme nonequilibrium electron transport in conventional device geometries can give rise to space

charging at the source and backscattering from the drain into the source. However, taking a contrarian view, suppose one were to design the device to exploit extreme nonequilibrium electron transport instead of treating it as a parasitic. This might pose challenges to materials, processing, and geometry, but, on the other hand, designing a device with extreme nonequilibrium electron transport in the channel and power dissipation in the drain might have superior thermal properties with potentially important consequences for thermal management of circuits.

The above examples are typical of a simple ad-hoc design methodology in which one identifies a difficulty in device design and then tries to create a solution. The result is a series of improvements heavily weighted towards incremental small changes from previous practical experience. This approach has worked successfully for many years and also applies to other aspects of system design. For example, one might anticipate that circuit designers, when faced with statistical variations in transistor threshold due to variation in lithographic and pattern transfer processes during chip manufacture, will develop methods that aim to effectively cancel such stochastic effects. Correlations in the behavior of adjacent transistors might be exploited to nullify variations in small circuits consisting of a few transistors. Likewise, rather than provide a limited number of transistor types, aspects of transistor design could be exposed to the circuit designer, enabling a better match of device performance to function.

Despite all the tremendous activity, one is, however, left with the uncomfortable feeling that maybe a better approach to solve a given problem has been ignored or inadvertently missed. Because of the large number of variables, it seems reasonable to consider avoiding ad-hoc design and trying to apply a systematic approach to problem solving and analysis. Such an approach is more likely to reap dividends as we move away from devices that behave semiclassically and into a less familiar quantum regime where our intuition might fail.

III. DESIGN IN THE QUANTUM AGE

In the quantum arena, the simple physical scaling of device geometry no longer provides a path to increased system functionality; rather device performance and functionality is achieved by manipulating new quantum degrees of freedom. Examples include controlling the single electron states of atomic and nanometer-sized particles via geometry [19], [20], using interacting electrons in the presence of the coulomb interaction to exploit collective excitations such as plasmons [21], hybridization to control bonding and chemical specificity, using electron and orbital spin to control magnetic response [22], strong light-matter interaction in nanometer-sized geometries [23], [24], and nonequilibrium processes on femtosecond time scales [25].

To date, much of what has been explored is the result of curiosity-driven science with little direct connection to practical technology development. This common approach to discovery may be not only inefficient but also susceptible to replacement by more effective methods.

In the future, it might be possible to reliably control the precise spatial positions of atoms, molecules, and nanoscale structures using the experimental techniques now being developed by nanoscience. To complement these emerging capabilities, it seems clear that a new set of design tools should be developed to assist in the exploration of a potentially vast number of atom and nanoscale configurations with a corresponding enormous range of physical properties.

A conventional approach to the design of nanoscale devices will likely miss many possible configurations. At the same time, it is unrealistic to expect individuals to manually explore the vast phase space of possibilities for a particular device function. It seems reasonable to consider using machine-based searches of configuration space to numerically identify the best broken-symmetry spatial arrangement that produces a desired response.

A. Control of Electron Transmission Through a Tunnel Barrier

As a prototype system, consider the $Al_xGa_{1-x}As$ material system. Atomically precise layer-by-layer crystal growth is possible using MBE, and the $Al_xGa_{1-x}As$ alloy can be used to form heterojunctions with controlled conduction and valance band offsets.

Fig. 2(a) shows a rectangular barrier of energy $V_0 = 0.3$ eV and thickness $L = 4$ nm. The n-type electrodes on either side of the barrier have carrier concentration $n = 10^{18}$ cm^{-3}. In accordance with the Poisson equation, application of a bias voltage V_{bias} depletes carriers in a region on the right side and accumulates carriers in a region on the left side of the barrier. Electron motion though the potential $V(x)$ is in the x-direction, normal to the barrier plane, and there is no confinement in the y and z directions. The absence of lateral confinement avoids restrictive design constraints imposed by quantized conductance [26]–[28].

Fig. 2(b) shows transmission probability $T(V_{\text{bias}})$ for the simple rectangular barrier as a function of V_{bias} for an electron of energy $E = 26$ meV incident from the left. As expected, there are resonances and a rapid increase in overall transmission with increasing V_{bias}. It is because of this that the design of structures with linear and other power-law transmission-voltage characteristics likely involves broken-symmetry potential barrier profiles.

Suppose one wishes to find a potential profile with a transmission function $T(V_{\text{bias}})$ that increases *linearly* with bias voltage in the range $0\ \text{V} < V_{\text{bias}} < 0.25\ \text{V}$. Fig. 3 shows the result of an exhaustive numerical search for a conduction band profile $V(x)$ that gives a linear $T(V_{\text{bias}})$ characteristic. The search for the optimal $V(x)$ is performed on a grid with $\Delta x = 2$ nm ($\sim$8 monolayers of GaAs) spatial increments and $\Delta V = 0.01$ eV energy

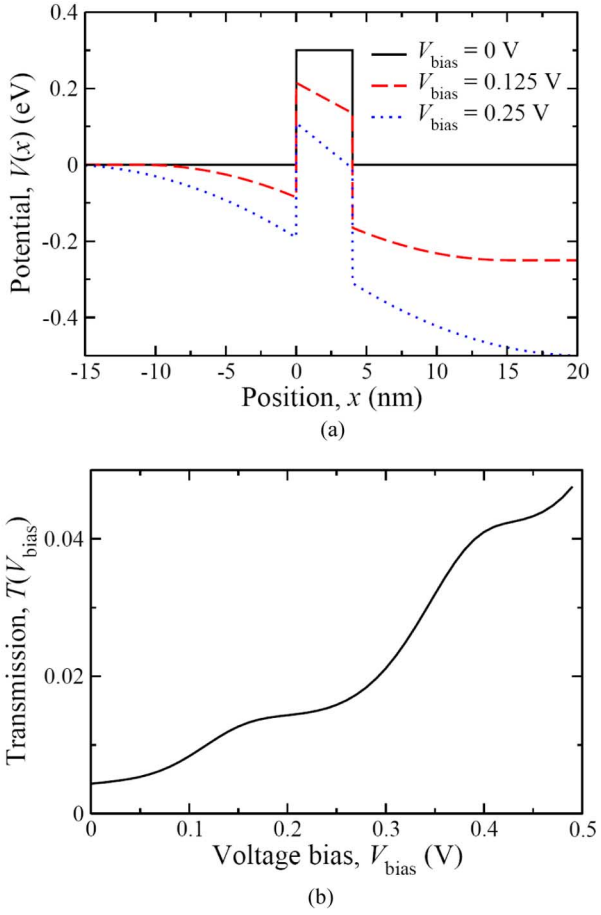

Fig. 2. *(a) A rectangular potential barrier of energy $V_0 = 0.3$ eV and thickness $L = 4$ nm gives rise to rapid increase in electron transmission with increasing voltage bias V_{bias} and resonances. Effective electron mass is $m = 0.07m_0$, where m_0 is the bare electron mass. (a) Conduction band profile of the rectangular potential barrier for the indicated values of V_{bias}. (b) Transmission probability as a function of V_{bias} for an electron of energy $E = 26$ meV incident from the left [29].*

increments. The barrier structure is limited to a total thickness $L = 10$ nm, and the maximum allowed on-site potential is 0.3 eV measured from the GaAs conduction band minimum.

The size of the nonconvex search space is large ($30^5 \approx 2.4 \times 10^7$). Each forward solve of the physical model takes about one second on an Intel Xeon processor with 3.2 GHz clock, 800 MHz front-side bus, 2 MB L2 cache, 2 × 1 GB ECC DDR-2 400 SDRAM, and running the Linux operating system. Calculations take less than five days on a cluster of 30 two-processor nodes at the University of Southern California high performance computing and communications (HPCC).[2]

As shown in Fig. 3, the optimal broken-symmetry conduction band profile $V(x)$ is nonintuitive, as are other less optimal designs. The nonconvexity of the solution space is well illustrated by the fact that the two next best designs in the exhaustive search have a quadratic deviation within 10% of the optimal design but belong to different local minima. The combination of a large search space and a nonintuitive conduction band profile supports the idea that device synthesis tools, such as those used to solve this design problem, can be employed to discover functionalities that would not be found by other means.

These and other results show it is possible to manipulate conduction band potential profiles to not only construct semiconductor nanoscale structures with desired linear and power-law electron transmission-voltage characteristics but also design current-voltage characteristics. In such devices, elastic scattering limits extreme nonequilibrium electron current flow and dissipative relaxation processes are spatially separated and

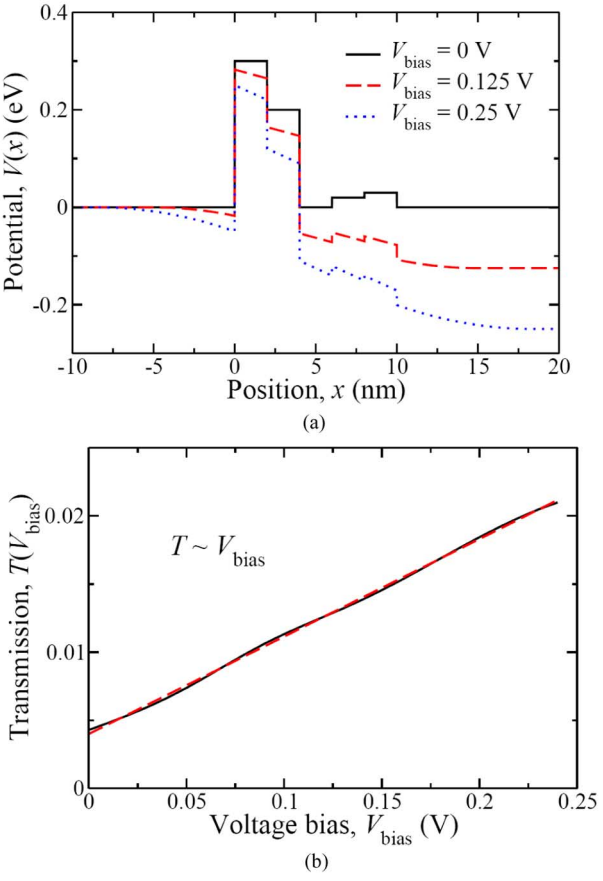

Fig. 3. *(a) Solution from an exhaustive numerical search for conduction band profile V(x) that yields a linear dependence of electron transmission as a function of bias voltage V_{bias}. V(x) is constrained to a region that is 10 nm wide, and the maximum local potential is 0.3 eV. The resulting $T(V_{bias})$ for an electron of energy $E = 26$ meV incident from the left are shown as a solid line in (b). Broken line is objective response. The quadratic deviation of the solution is $\chi^2 = 5.1 \times 10^{-7}$ [29].*

[2]http://www.usc.edu/hpcc/.

occur in the electrodes. This is very different from the physical mechanisms responsible for conventional devices exhibiting Ohms law in which current flow is impeded in the same region of space as dissipation takes place.

Large electric fields in nanoscale semiconductor devices can result in tunneling and nonequilibrium electron transport. While nonlinear devices such as transistors may take advantage of these phenomena, what has been demonstrated here is that it is also possible to create devices with linear response. Such devices are required because, for example, a linear resistor is a critical element for analog and low power circuit design. Optimal design has shown that linear response is not excluded by the exponential dependencies normally associated with electron tunneling in semiconductors.

Using these device synthesis results to learn more about the physics enabling power-law transmission as a function of V_{bias}, consider a progressive evolution of solutions for the linear objective from a simple square barrier to the multibarrier profile of Fig. 3(a). As illustrated in Fig. 4(a) and (b), the dominant transmission features of the simple square well, i.e., the exponential behavior and resonances, are altered by the addition of steps in the potential barrier profile. It is observed that the superposition of broad resonances due to the presence of different potential steps helps linearize the transmission-voltage curve. It is also this superposition of broad scattering resonances that renders the solution stable against small monolayer perturbations in barrier thickness and potential.

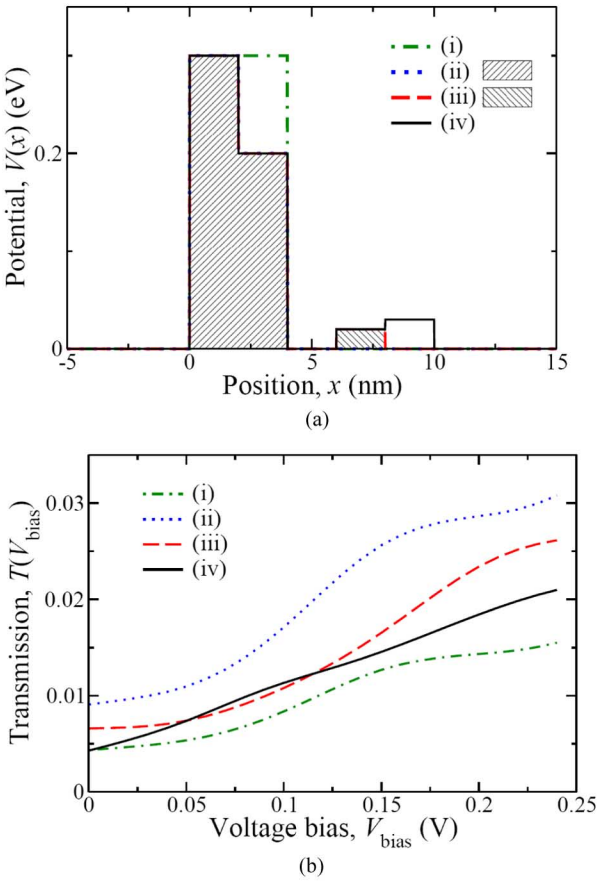

Fig. 4. *(a) Evolution from a single potential barrier to an array of barriers. (b) $T(V_{\text{bias}})$ for the potentials in (a). The superposition of broad resonances enables a linear transmission-voltage response. (i) Single rectangular barrier of 4 nm, (ii) 4-nm-wide barrier with a step, (iii) same as (ii) plus 1-nm-wide small barrier, and (iv) optimized potential profile [29].*

B. The Need for Improved Physical Models

The elementary barrier transmission problem discussed in the last section turned out to be quite rich in physical effects. However, it is obvious that the ability to discover useful new functions or improved performance will depend strongly on the realism of the physical model being used. For example, modeling the transfer characteristics of a bipolar transistor without including the possibility of inelastic scattering is unrealistic because the existence of base current flow requires such processes.

As a prototype physical system, scaled heterostructure bipolar transistors (HBTs) are particularly interesting. Compared to FETs, the inherently higher transconductance of HBTs allows greater current handling capability. From a manufacturing point of view, HBTs have the advantage that voltage threshold for current flow is controlled by the built-in base-emitter junction potential so that very uniform and reproducible device characteristics can be achieved. Both the high current handling capability and device threshold uniformity make HBTs suitable for high-performance analog circuitry [30]. In addition, control of the conduction band and valance band potential profile via epitaxial crystal growth techniques is a design degree of freedom that might best be exploited using a device synthesis methodology similar to that discussed in the previous section.

Today, a typical HBT design might make use of physical models of electron transport based on the Boltzmann transport equation or a semiclassical Monte Carlo method [31]–[34]. The reason why such semiclassical models are used is because they appeared to work in the past. Unfortunately, this approach is likely to fail as device dimensions shrink, internal electric fields grow, and nonequilibrium electron transport dominates device performance.

Conventional Boltzmann and Monte Carlo theories assume that collisions may be treated as isolated local events. The assumption of a local collision rate follows from the quantum kinetic theory of nonequilibrium Green's functions in slowly varying space and time potentials [35]–[37] and is often invalid in devices where scattering rates are large and/or memory effects are important. A further assumption is that scattering events are independent of the driving field/potential profile. This is incorrect if, before completion of each individual collision, other scattering processes occur or an electron gains so much energy from

the field during a collision that the collision process itself is altered. The latter is known as the intracollisional field effect [38]–[40] and typically becomes important for fields greater than 2×10^5 V cm^{-1}. When the characteristic time scale (the carrier transit time) is comparable to the collision time, as can occur in nonequilibrium electron transport, collisional broadening can no longer be ignored. Electron energy and wave vector become independent variables, and the relationship between them is described by a spectral density function. In fact, in most modern devices, the assumptions underlying the Boltzmann and Monte Carlo theories are invalid.

To give an indication why, consider what happens if one places an abrupt potential barrier in the collector arm of a HBT. Obviously, one expects quantum mechanical reflection to play an important role in determining device performance. Fig. 5 shows results of measuring common emitter current gain β with bias V_{CE} for the AlAs/GaAs structure sketched in the inset. It is apparent that there are strong resonances in β associated with quantization of energy levels in the 40-nm-thick base-collector region. Semiclassical arguments suggest that both elastic (impurity) and inelastic scattering in the collector and delta doped p-type base are responsible for the resonance minima not decreasing to values closer to $\beta = 0$. A semiclassical description of nonequilibrium electron transport leads one to believe that inelastic scattering rates in the base present a fundamental limit to transistor performance [41]. Thus, in an effort to quantify this limit, one might try to calculate scattering rates for perpendicular nonequilibrium electron transport across the two-dimensional plane of p-type dopants in the base. In addition to various other complications, these scattering rates cannot be evaluated independently of collector bias V_{CB}. In fact, since base and collector regions may no longer be treated separately, one should treat the structure as a single inhomogeneous anisotropic scatterer. Within linear response, this requires evaluation of the nonlocal dielectric response $\varepsilon(\mathbf{r}, \mathbf{r}', \omega)$ for the entire transistor structure. Even this first step towards an appropriate physical model is quite challenging [42].

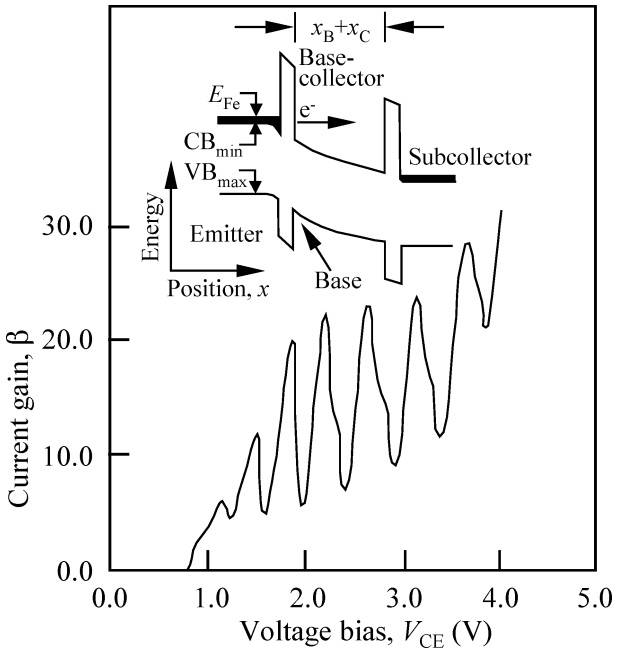

Fig. 5. *Measured current gain β with bias V_{CE} for the AlAs/GaAs HBT sketched in the inset. Lattice temperature is $T = 4.2$ K, emitter area is 5.8×10^{-5} cm^2, and base current is $I_B = 0.1$ mA. The AlAs tunnel emitter is 8 nm thick, the p-type base is delta doped with a Be sheet concentration of 6×10^{13} cm^{-2}, the AlAs collector barrier is 5 nm thick and emitter-collector barrier separation is $x_B + x_C = 40$ nm.*

In addition to the preceding, one expects quantum interference to become important in small-scale devices when significant changes in the carrier velocity occur on a length scale comparable to the particle wave length but short compared to its mean free path. In low effective electron mass semiconductors, this occurs for potential changes of greater than ~0.2 eV and length scales less than ~10 nm. The spatial potential profile, in which the electron moves, must then be treated quantum mechanically, thereby altering the states and scattering rates. Another important requirement becomes apparent by simply recognizing the fact that any model of electron transport in microstructures should not violate Maxwell's equations. Thus, one needs to be able to deal with the possibility of large dynamic space charging effects due to quantum mechanical reflection as, for example, occurs in a resonant tunnel diode. Not only can elastic quantum mechanical reflections from an abrupt change in potential strongly influence inelastic scattering rates but also dissipative processes can in turn modify quantum reflection and transmission rates. This type of feedback is driven by unitarity [43], [44]. Ultimately, what is needed is a new approach to describing quantum electron transport in modern devices to replace the old methods that are no longer either adequate or valid.

Today's practical problems in HBT design have roots in what has been discussed in this section. Current difficulties can be categorized into three areas, the first of which is efficient charge injection at the emitter to achieve high frequency response. The appropriate material composition and band edge profile for optimal emitter performance is unknown in part because it requires an optimal design for the complete transistor, which, in turn, requires a level of physically realistic model that does not exist at present. The second issue focuses on finding the best collector space charge region potential profile. This has a critical influence on collector delay and breakdown voltage. The third issue concerns the creation of degenerate minority carrier distributions under high drive current conditions and its influence on collector delay and breakdown voltage. New, more physically realistic models of electron

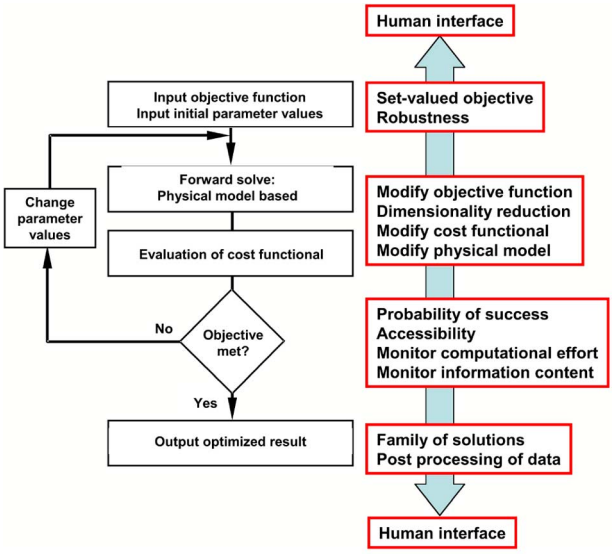

Fig. 6. ***Conventional optimization flowchart (left) and areas where additional adaptivity might assist in the exploration of solution space.***

transport in transistors are a prerequisite to future rationale design.

C. Advanced Optimization

The core task of optimal design is the numerical search of configurations resulting in global minima (or maxima) in solution space with respect to a user-defined objective function. Typically, a nonconvex solution space might consist of a shallow landscape with many local minima. Local measures of curvature around the minima might give an indication of robustness of a given solution with respect to small variations in control parameters. Applying these basic ideas to synthesize a device design, one might program according to the flowchart shown on the left in Fig. 6.

The input to the flowchart in Fig. 6 is the objective function and a set of initial parameter values. Initially, one might think that it is easy to specify the objective function; however, the fact of the matter is this is usually neither the case nor desirable. For example, one does not want to specify a particular transistor transfer characteristic that is inaccessible; rather one would prefer to be presented with a family of characteristics that are both accessible and insensitive to small variations in design parameters. As indicated on the right-hand side of Fig. 6, advanced optimization specifies a set-valued objective instead of a single objective. In addition, one will usually be concerned with the robustness of the solutions. The subject of robust optimization in a nonconvex solution space is today a focus of much research activity [45], [46].

Measures of distance can have a dramatic influence on the convexity of the cost function. Typically, a forward solve of the physical model is computationally expensive while evaluation of the cost function is not. Hence, calculating and comparing the performance of, and choosing between, different cost functions can be an effective strategy to improve efficiency.

Because, at least initially, the user probably does not know the best objective function to request, a feature of advanced optimization should also be its adaptivity. As indicated on the right-hand side of Fig. 6, inclusion of on-the-fly modification of the cost function, model, and related decision-making tools has the potential to create an adaptive optimization paradigm in which at the end of the calculation both the problem and the algorithm have changed.

IV. CONCLUSION

As the Moore's law era comes to a close, the possibility of technological surprise increases. In particular, control of material composition at the atomic scale has potential to dramatically increase electronic device design space in part due to quantum effects that provide vast new degrees of design freedom. As a step towards quantum engineering, synthesis tools and realistic physical models should be developed to efficiently explore the nonintuitive parts of this space and discover the best device designs for electronic systems. ■

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