Low-power 2.5 Gbps VCSEL driver in 0.5 μm CMOS technology

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Abstract

0.5μm CMOS technology is used to drive oxide-confined low-threshold current Vertical Cavity Surface Emitting Laser diodes at 2.5 Gbps. The 7 mW power consumption for the optoelectronic transmitter is twenty times less than a 3.6 V electronic Positive Emitter Coupled Logic transmit circuit and four times less than a 3.6 V electronic Low Voltage Differential Signal transmit circuit.

INRODUCTION

System-level integration based on electrical interconnects has failed to keep pace with the power, density, and signaling-speed improvements possible using scaled Complimentary Metal Oxide Semiconductor (CMOS) technology. Part of the reason for this is that it is difficult to increase the volume packing and edge-connection density (form-factor) at faster electronic signaling rates without incurring increased crosstalk, increased packaging cost, and increased power consumption needed to drive impedance controlled electrical interconnects [1 - 2].

High-speed electrical CMOS transmit circuits consume a significant amount of power. An individual differential CMOS Positive Emitter Coupled Logic (PECL) transmit circuit in 0.8 µm CMOS capable of operating at 2.0 gigabit per second (Gbps) from a 5 V power supply [3] consumes 120 mA from the power supply, 28 mA of which is returned to V_{TT} = 3.0 V at the receive side, to give a net circuit power consumption of 516 mW. The implementation of the transmit circuit in 0.5 µm CMOS for 3.6 V PECL signaling at 2.5 Gbps has a power consumption of 155.8 mW. The same circuit consumes 910 mW using a 5.0 V power supply. Migration to Low Voltage Differential Signal (LVDS) results in a 0.5 µm CMOS transmit circuit which occupies an area of 196 µm X 235 µm and whose power consumption is 30 mW for data rates up to 3.3 Gbps using a 3.6V power supply. Because of the differential nature of the analog circuit, power consumption is essentially the same at 1.25 Gbps.

Optical interconnects based on low-threshold current oxide-Vertical Cavity Surface Emitting Laser (VSCEL) diodes [4 - 5] offer a dramatic reduction in transmit circuit power consumption, which can advantageously offset the power consumption of a CMOS optical receiver while retaining the inherent bit-rate capacity, form-factor, and power advantages of the optical interconnect. In this letter we present initial experimental results which indicate that low-threshold current oxide-VCSEL diodes can be driven by low-power CMOS circuits at multi-Gbps rates with no errors.

RESULTS

Figure 1 shows an eye-diagram, schematic, and measured small signal response of an electrical Receive - Transmit (Rx - Tx) circuit that has been implemented in the 0.5 µm CMOS offered

through the MOSIS service. The Rx and Tx circuits satisfy the electrical requirements of the LVDS standard. The Rx circuit has integrated 50 Ω termination resistors. The Tx circuit is implemented as a differential current source driver with no source termination. The Rx and buffer circuits each consume 10 mA and the Tx circuit consumes 11.7 mA, 8mA of which is sent into the link (i.e., down the transmission lines into 50 Ω termination at V_{TT}). Measured electrical Bit Error Ratio (BER) tests of the circuit shown in Figure 1 indicate a data rate of 3.3 Gbps (300 ps bit period) for Vin = 200 mVp-p, Vdd = 3.60 V, V_{TT} = 1.75 V with BER < 1.0 X 10^{-12} is possible. At a BER < 10^{-3}, the measured eye-width of the output is 223 ps and the eye-height is 100 mVp-p. Rise and fall times of the electrical outputs are 116 ps and 160 ps respectively. The input sensitivity decreases to 50 mVp-p for input data rates below 3.0 Gbps. The power consumption of the complete electrical link is 99.76 mW (3.6 V X (10 mA + 10 mA + 3.7 mA) + (3.6 - 1.75) V X 8.0 mA = 99.76 mW).

The laser diodes available for the experiment are low-threshold current oxide-confined VCSELs from Hewlett Packard [5] with emission wavelength at λ = 850 nm. Laser diode L1 has threshold current I_{th} = 0.5 mA and threshold voltage V_{th} = 1.5 V. Laser diode L2 has I_{th} = 0.2 mA and V_{th} = 1.5 V. The positive output of the transmit circuit is used to drive the VCSEL and the negative output of the Tx circuit is connected to a sampling oscilloscope via a bias-tee. The optical output of the VCSEL is collected using a lensed multi-mode fiber and measured with an optical receiver which has a - 3 dB bandwidth of 1.67 GHz. The eye-diagrams in Figure 2 and 3 correspond to 2^{31} - 1 Non-Return-to-Zero (NRZ) Pseudo-Random-Bit-Stream (PRBS) 50 mVp-p input patterns. In these Figures, eye-widths and heights are measured at a BER < 1.0 X 10^{-3} and the displayed eye-diagrams have measured BER < 1.0 X 10^{-13}.

Figure 2 shows the electrical (lower trace) and detected optical (upper trace) eye-diagrams of the Tx circuit coupled to L1 and operating at 2.5 Gbps (400 ps bit period). The steady-state bias current of L1 is 1.932 mA at a voltage bias of 1.7 V. The measured average light output of L1 is 372 μW at this operating point. The signal current delivered into L1 has a measured peak-to-peak value of 1.6 mA. The detected optical output has an eye-width of 295 ps and an eye-height of 55 mV. The electrical output has an eye-width of 313 ps and an eye height of 163 mV. Figure 3

shows the electrical (lower trace) and detected optical (upper trace) eye-diagrams of the Tx circuit coupled to L2 and operating at 1.25 Gbps (800 ps bit period). The time averaged bias current of L2 is 0.48 mA at a voltage bias of 1.6 V. The measured average light output of L2 is 38.9 μW at this operating point. The measured signal current delivered into L2 is 336 μA peak-to-peak. The detected optical output has an eye-width of 614 ps and an eye-height of 138 mV. The electrical output has an eye-width 738 ps and an eye-height of 288 mV.

A differential Tx circuit delivering the 1.6 mA signal current required to drive L1 at 2.5 Gbps consumes 1.16 mA for the predriver and has a total power consumption of 7.22 mW, which is approximately one fourth of the power consumed by the Tx circuit for the LVDS electrical case. A differential Tx circuit delivering the 336 μA signal current required to drive L2 at 1.25 Gbps consumes 242.6 μA for the predriver and has a total power consumption of 1.50 mW.

Our experimental results indicate that compared to LVDS, the power consumption of the CMOS optical Tx circuitry can be reduced by a factor of better than 4 while driving the low-threshold current oxide-VCSEL L1 at 2.5 Gbps and by a factor of 20 while driving the low-threshold current oxide-VCSEL L2 at 1.25 Gbps. The measured electrical sensitivity of the electrical Rx circuit is 50 mVp-p at 2.5 Gbps and 10 mVp-p at 1.25 Gbps. This implies that a 975 Ω transimpedance amplifier for the case of L1 and a 1860 Ω amplifier for the case of L2 is required for a complete CMOS optoelectronic link, assuming a conversion efficiency of 0.55 for the photodiodes and an optical link-loss of 6 dB.

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References:

[1] NORDIN, R. A., LEVI, A. F. J., NOTTENBURG, R. N., O'GORMAN, J., TANBUN-EK, T., and LOGAN, R. A.: 'A systems perspective on digital interconnection technology', J. Lightwave Technol., 1992, **10**, pp. 811-827.

[2] KRISHNAMOORTHY, A. V., MILLER, D. A. B.: 'Scaling Optoelectronic-VLSI Circuits into the 21st Century: A Technology Roadmap', IEEE Journal of Selected Topics in Quantum Electronics, 1996, **2**, pp 55 - 76.

[3] SANO, B., MADHAVAN, B., and LEVI, A. F. J.: '8 Gbps CMOS interface for parallel fiber-optic links', Electron. Lett., 1996, **32**, pp. 2262-2263.

[4] YANG, G. M., MACDOUGAL, M. H., DAPKUS, P. D.: 'Ultralow Threshold Vertical Cavity Surface Emitting Lasers Obtained with Selective Oxidation', Electronics Letters, 1995, **31**, pp 886-888.

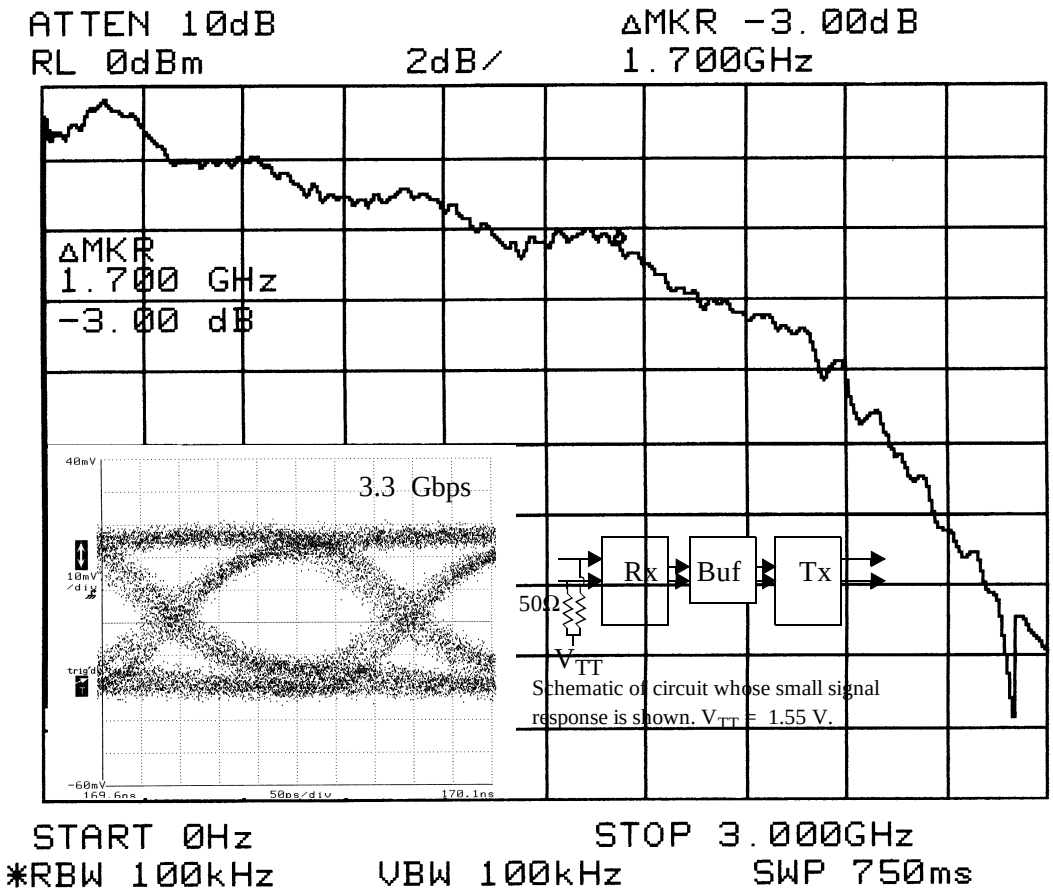
[5] SCHNEIDER, R. P., TAN, M. R. T., CORZINE, S. W., and WANG, S. Y.: 'Oxide-confined 850 nm vertical-cavity lasers for multimode-fiber data communications', Electron. Lett., 1996, **32**, pp. 1300-1302.

Figures:

Figure 1: The main figure shows the small-signal response of a circuit whose schematic is shown in the inset on the right, which has been implemented in 0.5 μm CMOS. The -3 dB small-signal response is 1.7 GHz. The inset on the left shows the eye-diagram of the Rx - Tx circuit for 200 mV input amplitude 3.3 Gbps 2^{31} - 1 NRZ PRBS. Vertical scale is 200 mV/div and horizontal scale is 50 ps/div.

Figure 2: Upper trace shows detected output of VCSEL L1 driven by positive output of Tx circuit. Lower trace shows negative output of Tx circuit. Input data is 50 mV 2.5 Gbps 2^{31} - 1 NRZ PRBS.

Figure 3: Upper trace shows detected output of VCSEL L2 driven by positive output of Tx. Lower trace shows negative output of Tx circuit after 20 dB attenuation prior to display. Input data is 50 mV 1.25 Gbps 2^{31} - 1 NRZ PRBS.



Schematic of circuit whose small signal response is shown. V_{TT} = 1.55 V.

Figure 1

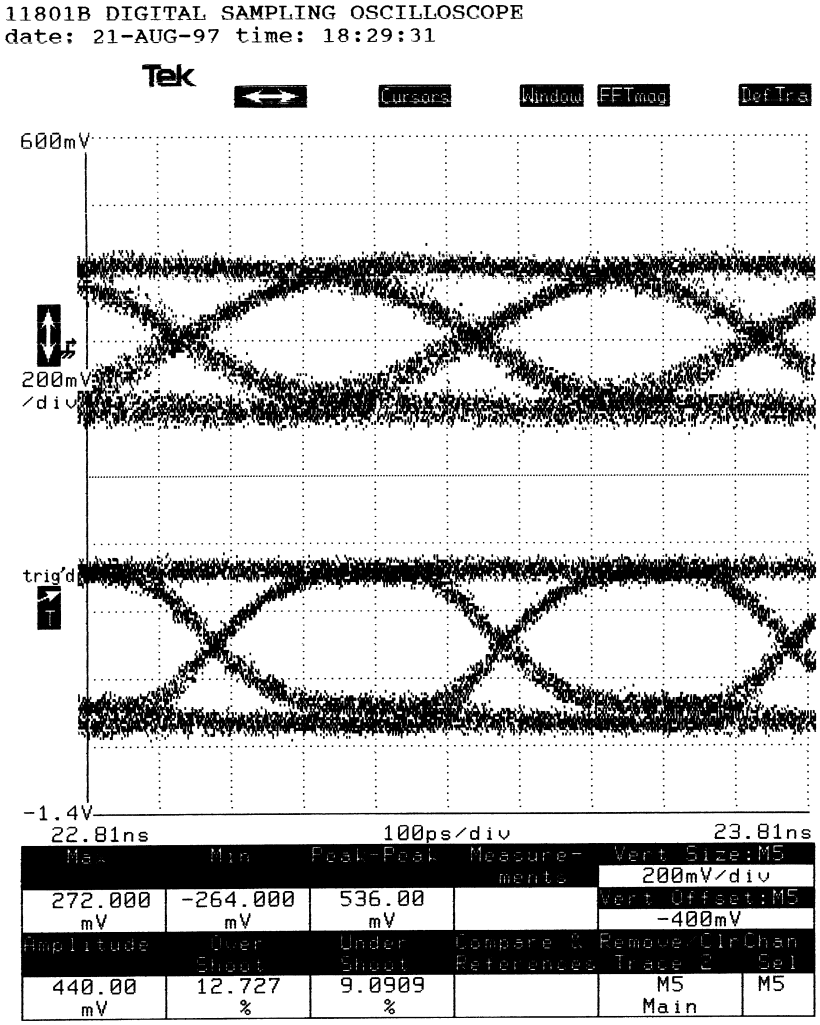

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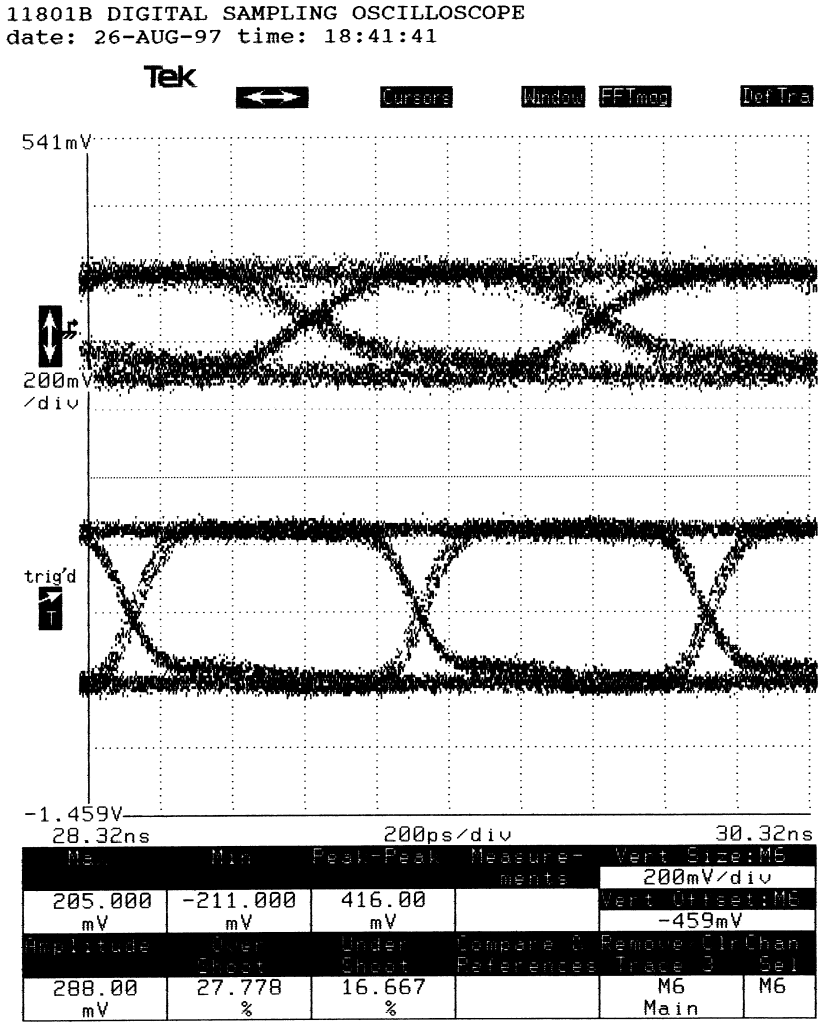
Figure 2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Min
Peak-Peak
Measurements
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-211.000 mV
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Amplitude
Over Shoot
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27.778 %
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Figure 3