Expitaxial metal–semiconductor structures and their properties

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(Received 4 June 1986; accepted 7 August 1986)

Recent development of epitaxial silicide technology has allowed structurally perfect metal–semiconductor interfaces to be fabricated. The atomic structure at these abrupt silicide–silicon interfaces has been modeled and electron transport across Schottky barriers with homogeneous interface structure have been studied for the first time. In addition, high quality multilayered structures of epitaxial metals and semiconductors have been fabricated, opening up possibilities for very high speed device applications. This paper reviews the state-of-the-art growth techniques, and the novel structures and properties of single crystal silicide thin films and multilayers.

I. INTRODUCTION

In the last decade, metal silicide thin films have attracted a great deal of interest in the semiconductor industry.[1] In particular, considerable scientific effort has been directed towards exploring the growth of epitaxial silicide films and the physics associated with their unique and novel structures.[2,3,4] Epitaxial silicide–silicon systems have thus far been demonstrated to be the closest to stucturally perfect and abrupt metal–semiconductor junctions in existence.[5] For instance, they are far superior in structure to epitaxial metal-compound semiconductor systems, where the interfaces are usually broad and graded over many lattice spacings due to chemical reactions.[6] Interest in epitaxial metal–semiconductor systems over nonepitaxial systems stems from two areas. On one hand, the perfection of the epitaxial structures offers a unique opportunity to study the physics at metal–semiconductor interfaces.[5] For example, the atomic structure at the interface may be modeled by state-of-the-art high resolution electron microscopy and the formation of a Schottky barrier (SB) at such a structurally "perfect" metal–semiconductor junction may be studied in a systematic way. Correlated with the homogeneous interface structure, such electrical studies are in fact the first microscopic studies of a metal–semiconductor junction.[7] On the other hand, epitaxial metal–semiconductor multilayers offer the possibility of novel device applications which are not available using nonepitaxial structures. For instance, they are an essential building block in the development of three-dimensional integration technology. Moreover, certain unique structures which may have exciting transport behavior can only be fabricated with the use of epitaxial silicides.

The rapid progress in this field owes its success to the utilization of ultrahigh vacuum (UHV) techniques and the careful control of the processing parameters. Operated in an essentially impurity-free environment and guided by various surface analytical techniques, the reaction of monolayers of metal with silicon has been studied in detail, leading to the development of unusual fabrication techniques for particular silicide–silicon systems.[8] Only two silicides, $NiSi_2$ and $CoSi_2$, have been demonstrated to establish single crystal, homogeneous interfaces with Si. In this paper, we will limit our discussions to structures consisting of ultrathin (< 100 Å) layers of these two silicides, as these are of the most interest to the scientific and technological communities. Epitaxial metal–semiconductor structures with thicker layers have recently been reviewed.[9]

II. GROWTH OF THIN SILICIDE LAYERS IN UHV

A. $NiSi_2$ on Si(111)

The reaction of monolayers of nickel with the Si(111) surface at room temperature has been studied using various techniques.[10–12] It is clear that considerable intermixing occurs between the first few monolayers of deposited nickel and the silicon substrate even at room temperature, although the structure of the disordered "silicide phase" is still not known. When such a precursor structure is annealed to $\sim$450–500 °C for a short period of time, epitaxial $NiSi_2$ layers with a remarkable degree of perfection can form, with the orientation of the layer dependent on the original nickel thickness.[8] Type A oriented $NiSi_2$ has identical orientation as the substrate, while type B oriented $NiSi_2$ shares the [111] axis with the substrate but is rotated 180 ° about this axis with respect to the Si.[7]

The variation of $NiSi_2$ orientation as a function of deposited Ni thickness is shown in Table I. Using deposited nickel at room temperature, at a rate of $\sim$0.5–2 Å/s, and subsequent annealing of $\sim$450–500 °C for $\sim$1 min, the dependence of $NiSi_2$ orientation on the nickel thickness is reproducible. Thin layers formed with either 1–5 Å Ni or $\sim$9–11 Å Ni are type B oriented and those with 16–20 Å of Ni are type A oriented. $NiSi_2$ layers grown with other deposited nickel thickness contain mixed type A and type B grains. Transmission electron microscopy (TEM),[5] low-energy electron diffraction (LEED),[8] Rutherford backscattering spectrometry (RBS), and channeling[13] have been used to study the orientation of these thin layers. No misfit dislocations are observed in the thin type A $NiSi_2$ layers, indicating the growth to be essentially pseudomorphic. There is usually a low density of misfit dislocations at the type B $NiSi_2$ interface. Type A layers and type B layers thicker than $\sim$30 Å are very uniform according to TEM observations. Dark-field planview TEM images of selected thin $NiSi_2$ layers are shown in Fig. 1. The interfaces of these layers are locally sharp and uniform as described previously.[5] The structure of the thin-

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TABLE I. Orientations of thin $NiSi_2$ layers on Si (111).

Deposition of (Å)	Deposition rate (Å/s)	Onto surface of	Deposition temperature (°C)	Annealing at (°C)	Orientation of $NiSi_2$	Remark
~1–5 Ni	~0.5–2.0	Si(111)	RT[a]	~500	B[c]	
~6–8 Ni	~0.5–2.0	Si(111)	RT	~500	A + B	
~9–11 Ni	~0.5–2.0	Si(111)	RT	~500	B	
~12–14Ni	~0.5–2.0	Si(111)	RT	~500	A + B	
~16–20 Ni	~0.5–2.0	Si(111)	RT	~500	A	
>24 Ni	~0.5–2.0	Si(111)	RT	~500	A + B	
~8–11 Ni	~0.1–0.2	Si(111)	RT	~500	B	
~13–30 Ni	~0.1–0.2	Si(111)	RT	~500	A + B	
~14–50 Ni	~1.5	Si(111)	RT	~500[d]	A	
$NiSi_x$, $x\sim2$ (co-evap.)	u[b]	Si(111)	RT	~500	B	
n Ni + mSi sequentially $m\sim3n$	u	Si(111)	RT	~500	B	
Ni	u	Si(111)	500–600	···	A + B[c]	MBE
$NiSi_x$, $x\sim2$	~1–5	Si(111)	500–600	···	B	MBE
~4 Ni	u	$NiSi_2$	RT	~500	same as[e] original $NiSi_2$	
~13 Ni	u	type B $NiSi_2$ (from 4 Å Ni)	RT	~500	A	

[a] RT denotes close to room temperature.
[b] u denotes unimportant.
[c] Islands.
[d] Fast heating rate.
[e] Not reproducible if original $NiSi_2$ thickness is < 25 Å.

nest (< 20 Å average thickness) type B layers is more complicated, consisting of a very thin layer of type B $NiSi_2$ (a triple layer ~3.1 Å thick) covering the majority of the surface and, in addition, three-dimensional $NiSi_2$ islands.[8,5]

The most reliable method for determining the orientation and the morphology of the silicide layers is a combination of TEM plan-view and cross-section imaging. Symmetry of the LEED pattern is also a reliable and sensitive technique for this purpose. This method makes use of the fact that the surfaces of type A and type B $NiSi_2$ are 180° rotated from each other and the fact that the intensity of (1, 0) type beam is nearly zero at ~84 eV for a singly oriented $NiSi_2$ layer (see Fig. 2 for selected single crystal LEED patterns). The symmetry of the LEED pattern at this particular energy is therefore, a good indicator of the layer orientation. Shown in Fig. 3 are the LEED patterns of a pure type A $NiSi_2$ layer and an essentially type B layer with ~5% of the area occupied by type A material. This demonstrates that LEED is a very convenient technique for silicide orientation determination with a detection limit of better than a few percent. The minimum for (1, 0) type beam at ~84 eV and the minimum for (0, 1) type beam at ~60 eV for single crystal $NiSi_2$ surface (see Fig. 2) are in very good agreement with a LEED intensity calculation based on a surface with a top Si layer.[14]

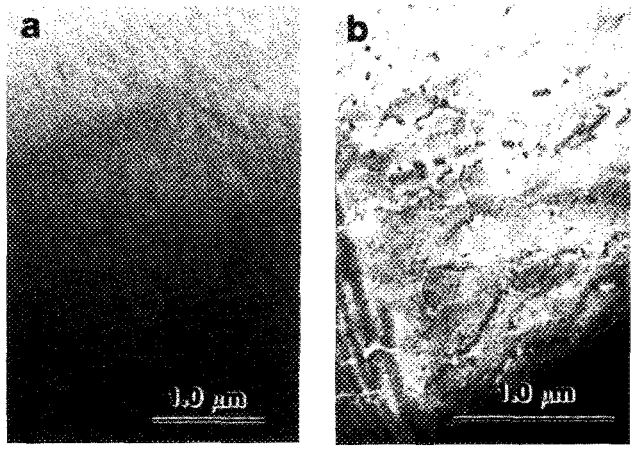

FIG. 1. Dark-field TEM images of (a) a type A $NiSi_2$ layer and (b) a type B $NiSi_2$ layer. These two ~65 Å thick template layers were grown by deposition of (a) ~18 Å Ni and (b) ~18 Å Ni and ~50 Å Si, respectively, on Si(111) at room temperature and subsequently annealing to ~500 °C for ~1 min. Mottled contrast in the upper part of (a) is due to damage in the thinning process.

An examination of Table I reveals that the silicide orientation depends critically on the details of the preparation. Variation in annealing procedure, deposition conditions, and wafer preparation can lead to modification of the curve describing the silicide orientation as a function of nickel thickness, as we originally published.[8] Usually, a faster deposition rate and an immediate annealing step favor the formation of type A orientation. Slower procedures help to obtain type B layers. A small wafer misorientation also favors the formation of type B $NiSi_2$. These observations suggest that the $NiSi_2$ epitaxial orientation depends on the kinetics of the reaction. This may have to do with the fact that the morphology and stoichiometry of the as-deposited "silicide" layer depends on the deposition rate of nickel. This is clearly demonstrated in AES analyses of room-temperature-deposited nickel layers.[15] Because of the dependence of silicide

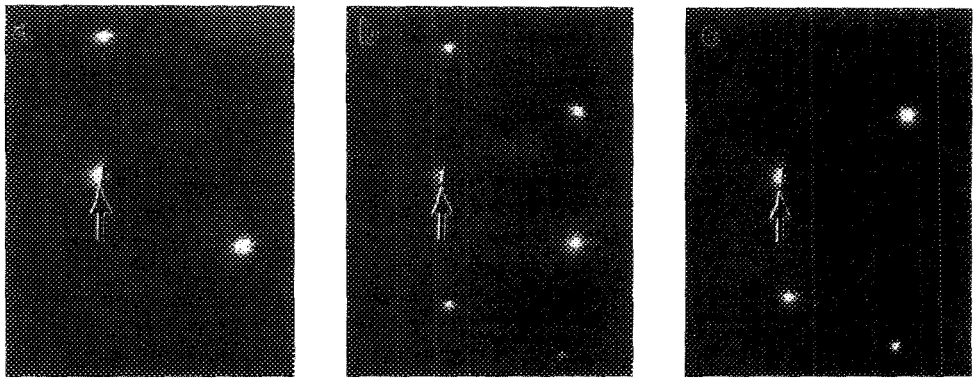

FIG. 2. LEED patterns of a ~65 Å type A $NiSi_2$ surface. Arrows indicate the positions of the (0, 0) beam. Incident electron energies: (a) 60 eV; (b) 71 eV; and (c) 84 eV.

orientation on the exact processing conditions, in any study of the various properties of thin $NiSi_2$ layers of a particular orientation, not only should great care be taken to exactly follow the growth condition for that orientation, but also some independent verification is required. The reaction temperature for the formation of ultrathin (<100 Å) $NiSi_2$ layers should not exceed ~650 °C, as silicide layers become unstable above this temperature. Auger analyses indicate a gradual decrease of nickel from the surface region and RBS shows a broadening of the tail of the nickel signal as well as a partial loss of epitaxy. High temperature annealing (>850 °C) is known to rid of as much as 500 Å $NiSi_2$ from the surface, presumably from nickel diffusion into Si and precipitation away from the surface.

The dependence of silicide orientation on the deposited Ni thickness is very intriguing. As may be seen from the table, there are many variations to the techniques for type B single crystal fabrication. For example, when a suitable layer of Si is deposited following, or concurrently with, the room temperature Ni deposition, an annealing to ~450 °C results in type B formation for the entire Ni thickness range (1–30 Å) investigated. In our original publication on ultrathin epitaxial $NiSi_2$/Si(111) formation,[8] we speculated on the reason for the observed dependence of silicide orientation on nickel thickness. The explanation offered evolved around three key factors: the structure of the as-deposited disordered phase; the interface free energies of the two orientations; and the kinetics of the reaction.[8] Since that time more experimental data have been gathered all of which seem to support our original model. This model has recently been described in detail.[9]

When a small amount of Ni (2–4 Å) is deposited on top of the thin $NiSi_2$ layers, the sharp 1×1 LEED patterns change to a diffuse $\sqrt{3}\times\sqrt{3}$. Upon annealing to ~450 °C, the sharp 1×1 pattern (with the same symmetry as before the nickel deposition) reappears. These LEED results and TEM analyses both show that such procedures increase the thickness of the $NiSi_2$ layers while maintaining the original silicide orientation. This procedure, if repeated enough times, is one way of growing a layer of $NiSi_2$ of any desired thickness with the predetermined orientation of the original $NiSi_2$ "template" layer. There is, however, a limit to the amount of nickel that may be deposited on top of the $NiSi_2$ template layer, if following the anneal the orientation of the original template layer is to be preserved in the new layer. This limit depends upon the original template thickness and morphology. Starting with a thin, uneven, type B (<20 Å average thickness) layer, such a procedure does not always yield pure type B layers.[16] The type B skin layer (~3 Å thick triple layer as described in a previous section) can easily be consumed through reaction with Ni to form metal-rich silicide, and $NiSi_2$ may have to renucleate. Mixed layers of A and B orientation are occasionally observed as a result.[16] There are much more convenient ways to increase the $NiSi_2$ thickness by use of thin templates.[17]

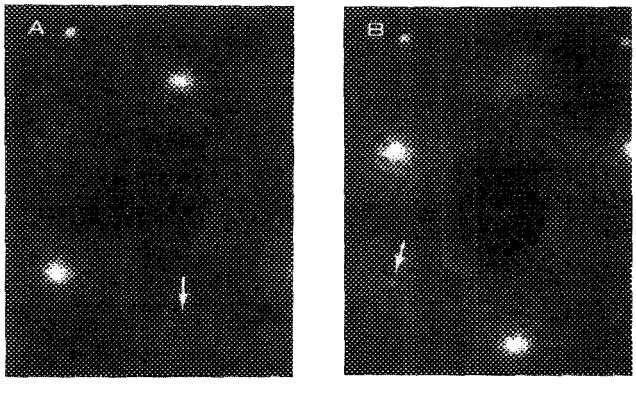

FIG. 3. LEED pattern of the surface of (a), a pure type A oriented $NiSi_2$ layer and (b), an essentially type B layer with ~5% of the area covered by type A material. The intensity of the arrowed spots gives an indication of the percentage of area occupied by silicide of the opposite orientation.

B. $NiSi_2$ on Si(100)

Reaction between monolayers of nickel with the Si(100) surface has been studied extensively in recent years. It is clear that reaction occurs even at room temperature.[10,18] As in the case of nickel reaction on Si(111), the intermixing appears to be self-limiting, ending after a few monolayers of deposited nickel. The morphology of the $NiSi_2$ layers grown from reacting monolayers of nickel deposited at room temperature on Si(100) depends on the nickel thickness.[8] Surfaces formed after annealing ~10–20 Å of Ni display reconstructed LEED patterns similar to those reported for the $NiSi_2$(100) surface.[19] An example taken from the surface of a layer grown by reacting 14 Å of Ni is shown in Fig. 4(a). LEED patterns found on surfaces annealed with either >30 Å or <10 Å of nickel consist of this pattern and, in addition,

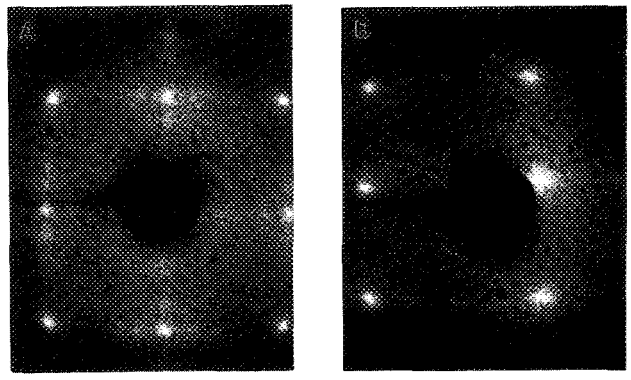

FIG. 4. LEED patterns of single crystal $NiSi_2$ layers grown on (a) Si(100) and (b) Si(110), respectively.

1/2 order spots. This suggests a surface of $NiSi_2$(100) plus some area of bare Si(100). High resolution TEM images of $NiSi_2$ layers grown with different nickel thickness clearly confirmed the LEED results. In the thickness range of ~10–20 Å Ni, the silicide–Si interfaces are uniform and flat. Outside of this thickness range, inclined {111} facets are observed and the interfaces are very nonuniform with large exposed Si regions. Based on a nonuniform structure as the latter, LEED results and photoemission results can be simply explained without invoking any novel lattice structure.[20]

As in the case of the reaction on Si(111), the uniformity of reaction $NiSi_2$(100) layers also varies slightly with deposition and annealing conditions. This suggests that the extent of the precursor reaction plays a role in deciding the eventual silicide morphology.

C. $NiSi_2$ on Si(110)

Thin epitaxial layers of $NiSi_2$ may be grown on Si(110) and employed to fabricate thick single crystal $NiSi_2$ layers.[21] LEED patterns of the $NiSi_2$(110) surface may be used as an indicator of the continuity of the silicide layers, as in the case of the (100) surface. A LEED pattern of the unreconstructed surface of a continuous $NiSi_2$ thin layer on (110) is shown in Fig. 4(b). When the layers are not continuous, 2×1 reconstructed beams may be observed in addition to the silicide patterns. The most uniform $NiSi_2$ layers are grown with a deposited Ni thickness of ~15 Å. However, unlike templates formed on (111) and (100) surfaces, channeling through these layers is poor. This is because, even for these ultrathin layers, the interfaces consist mainly of {111} facets and the layers are strained by dislocations which necessarily reside at the boundaries of the facets.[21]

D. $CoSi_2$ on Si(111)

The reaction of monolayers on cobalt with Si(111) at room temperature has not been studied as completely as the Ni reaction. However, there is already evidence for silicide formation at low coverages.[22,23] Type B orientation is observed for the majority of thin silicide films regardless of the growth conditions. Areas occupied by type A regions vary according to the exact preparation. Openings in the silicide films can always be found, although the density and size of these depend on the processing conditions.[24] Even at an

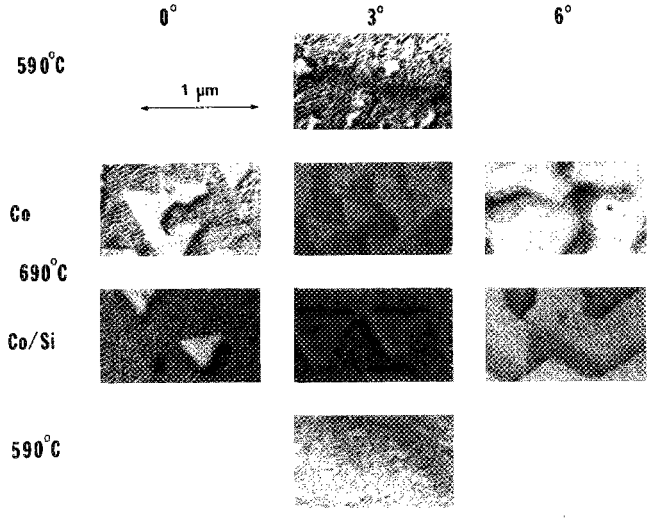

FIG. 5. Two-beam bright-field TEM images of various thin $CoSi_2$ films on Si(111). Co/Si and Co refer to the presence or absence of a Si layer deposited at room temperature along with Co; 590 and 690 °C refer to the silicide annealing temperature; 0^0, 3^0, and 6^0 refer to wafer miscut from (111).

average film thickness of only 50–100 Å, there is a network of misfit dislocations whose density is less than but comparable to those occurring for thick (~1000 Å) $CoSi_2$ layers. Shown in Fig. 5 are two-beam bright-field images of various thin $CoSi_2$ films on Si (111). Pinholes appear as areas from which Moiré fringes are absent. Moiré fringes arise from the misfit dislocation network primarily between the substrate Si and $CoSi_2$ layer. Some pinholes are triangularly shaped with sides in the ⟨110⟩ direction. This direction arises from the inclined ⟨111⟩ facets which occur at the edges of the pinholes.

Growth conditions which have been shown to have a significant effect on pinhole distribution are film thickness, composition of the deposited film (Co/Si ratio), substrate orientation, annealing conditions, etc. To grow the most uniform $CoSi_2$ layers it is necessary to use ratios of Co/Si~1, temperatures of less than 600 °C, substrates cut to exactly (111) orientation, and $CoSi_2$ thicknesses of ~60–90 Å. Any departure from these conditons results in an increase in the size and density of the openings. For instance, high annealing temperature and long annealing time result in silicide films with large holes, similar to the case with thick silicide layers.[25,26] Room-temperature deposition of a thin Si layer following the Co deposition helps to reduce the size and density of openings as well as nearly eliminate the type A $CoSi_2$ grains. Symmetry in the LEED pattern of the surface may also be used to give a quick yet reliable estimate of the orientation of the silicide layers. LEED patterns of the surface of an essentially pure type B layer and a layer of majority type B with a small fraction of type A orientation as well as exposed 7×7 Si regions are shown in Fig. 6. These two layers were grown by annealing a deposited Co/Si film and a pure Co thin film, respectively. Annealing of a mixed Co/Si deposited film helps in achieving a more peaked distribution of pinhole sizes in the silicide layer on a miscut (111) surface. With miscut Si(111) substrates, larger openings are observed.

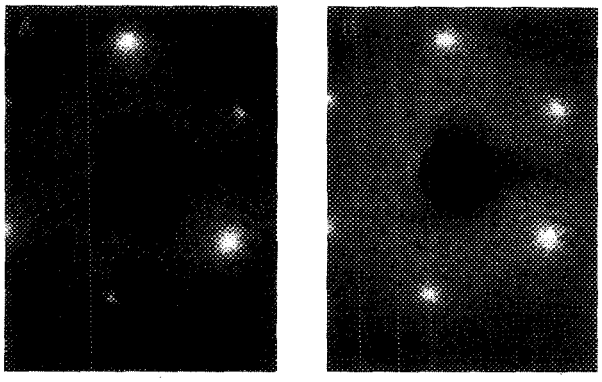

FIG. 6. LEED patterns of the surfaces of (a) an essentially continuous pure type B $CoSi_2$ layer and (b) a majority type B $CoSi_2$ layer with observable type A mixture and openings on Si(111).

The most uniform and continuous $CoSi_2$ films grown on Si(111) contained essentially no type A oriented grains and the size of the pinholes was very small, less than ~ 100 Å.[24] We have not, under any circumstances, observed $CoSi_2$ layers to be free of misfit dislocations or pinholes. These observations are in agreement with the findings of a recent work by Hunt *et al.*[27] Recently, however, using similar growth conditions, the growth of dislocation-free, pinhole-free $CoSi_2$ layers on Si(111) has been reported by D'Anterroches and co-workers.[28,29,30]

III. PROPERTIES OF EPITAXIAL SILICIDES

A. Interface atomic structures

Cherns *et al.*[31] first proposed two models for the atomic structure at $NiSi_2$/Si(111) interfaces, the so-called sevenfold and the fivefold structures. The names refer to the coordination numbers of the atoms contained in the first metal layers at the interface. The sevenfold model was found to agree with TEM images obtained for both type A and type B orientations in reacted mixed A + B samples.[31] The same conclusion was deduced from high resolution TEM studies of single crystal type A and type B thin layers.[5] However, the TEM images of the interfaces of type B $CoSi_2$ with Si(111) appear to agree better with the fivefold structural model.[32] However, some uncertainty surrounds the TEM data on $CoSi_2$ due to the possibility of stress relaxation in thin samples.[33] Further experiments are necessary to establish the details of the $CoSi_2$/Si interface.

The interfaces of epitaxial silicides grown on (111) substrates appear to be very abrupt, locally occurring within one interatomic spacing. On (100) substrates, although the interface is very uniform, some areas of the interface appear to have a finite width of several (200) planes, suggesting a high density of steps. High resolution TEM images of $NiSi_2$/Si(100) interfaces agree with a simple sixfold coordinated model of atomic structure.[5,34] Models of these silicide–silicon interfaces may be found in the literature.[5] It should be pointed out that these models were obtained by measuring the rigid shifts across the interfaces. The accuracy of such measurements is ~ 0.3 Å under axial bright-field imaging conditions with currently available high resolution instruments.[35] Small relaxation (< 0.3 Å) of the atomic positions near the interface cannot be ruled out from these studies. A recent ion channeling study suggests a small contraction at the type B $NiSi_2$/Si(111) interface.[36]

B. Schottky barrier heights

The formation mechanism of Schottky barrier heights (SBH) has not been established despite extensive investigation in recent years. A major obstacle has been the lack of direct experimental information correlating the SBH with relevant interface physical parameters. With the perfection of the epitaxial silicide structures, abrupt single crystal metal–semiconductor systems are available for the first time. So far, only the interfaces of $NiSi_2$ and $CoSi_2$ are found to have homogeneous atomic structure. Studies of electronic properties at these "ideal" SB junctions should provide much needed information regarding the possible relationship between local electronic and structural properties. SBH's of type A and type B $NiSi_2$ layers on Si(111) have been studied in detail.[7,16] SBH of type B $NiSi_2$ on *n*-type Si(111) is found to be higher by ~ 0.14 eV than that for type A $NiSi_2$. Shown in Fig. 7 are *C–V* plots of two $NiSi_2$ diodes measured at three different frequencies. Richardson's plots for a type A and a type B $NiSi_2$ layer grown on *p*-type Si(111) are shown in Fig. 8. Electrical behaviors were found to agree with those expected of an ideal metal–semiconductor junction, namely, a long and straight linear relationship for $\log I$ and $1/C^2$ plots from *I–V* and *C–V* measurements and good ideality factors for *I–V* traces. SBH's determined from *I–V*, *C–V*, and activation energy studies are all in good agreement with each other. No dependence on substrate doping was observed. The sum of SBH's on *p*-type substrate and those on *n*-type substrate are very close to the silicon band gap for either silicide orientation. SBH of single crystal $NiSi_2$ on Si(100)[37,38] and type B $CoSi_2$ on Si(111)[39,40] have also been investigated. These results are summarized in Table II.

The most striking result deduced from single crystal metal–semiconductor junctions is the variation of SBH with the

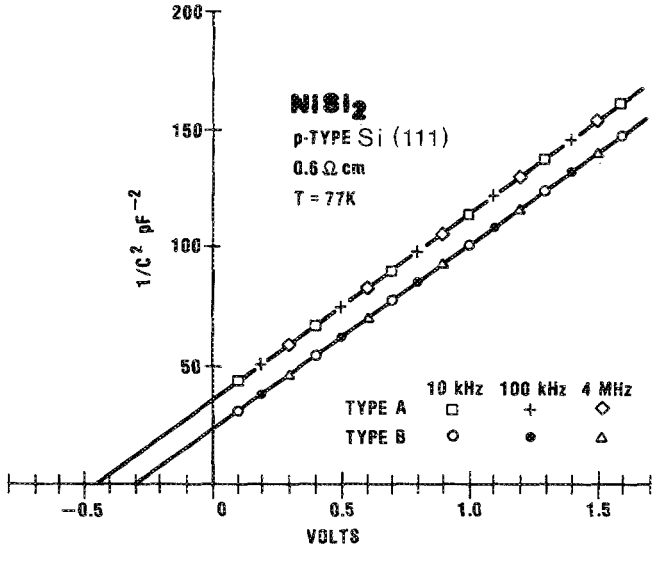

FIG. 7. Capacitance–voltage plots of a type A and a type B $NiSi_2$ diodes grown on *p*-type Si(111). Capacitances were measured at three different frequencies.

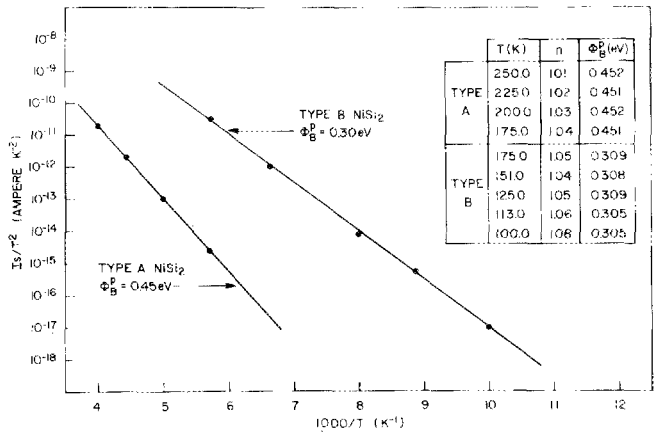

FIG. 8. Richardson's plots of the saturation currents obtained from forward I–V analyses of a type A and a type B $NiSi_2$ Schottky diode on p-type Si(111). SBH's (uncorrected for image lowering) and ideality factors at individual temperature are tabulated. SBH's determined from the activation energy method are also indicated.

silicide orientation. There is a significant difference between SBH's on Si(111) and (100). It is especially interesting to note that on Si(111) the SBH of type A $NiSi_2$ differs by $\sim$0.14 eV from that of type B $NiSi_2$. This variation of SBH on orientation has not been observed on polycrystalline metal–semiconductor systems. Neither is it predicted by any existing theory. So far, there has not been a satisfactory explanation of this effect. Generally speaking, if only one SB mechanism is responsible for the silicide SBH, such a dependence of SBH on crystal orientation would favor intrinsic electronic states as the SB mechanism. However, if one considers the possibility of more than one SB mechanism, then the answer is not as obvious. We believe that studying the electrical properties of single crystal metal–semiconductor systems and paying attention to the details of the interface structure may lead to direct identification of the SB mechanism. The interfaces between single-crystal silicide and silicon remain the closest to ideal, simple, and well-controlled systems for that purpose.

Recently, Liehr *et al.*[41] reported SBH's for type A and type B $NiSi_2$ layers which were in disagreement with our results. A possible explanation for the apparent discrepancies has recently been pointed out.[16] The experimental procedure employed by Liehr *et al.*[41] of annealing the Si substrate to a high temperature in vacuum is known to induce the formation of a surface p-n junction.[16,42] This p-n junction can dominate the electrical transport behavior perpendicular to the interface and render results irrelevant to the position of the interface Fermi level. This high temperature annealing procedure should therefore be avoided in any studies involving SBH determination. Under careful experimental conditions where no doping compensation occurs, the dependence of SBH on the orientation of the silicide is very reproducible[16] and has recently been confirmed independently by another group.[43,44]

TABLE II. Schottky barrier heights of single-crystal silicide layers on n-type silicon.

Silicide	Orientation	Substrate	SBH(eV)
$NiSi_2$	A	(111)	0.65
$NiSi_2$	B	(111)	0.79
$NiSi_2$	···	(100)	0.48
$CoSi_2$	B	(111)	0.64

IV. GROWTH OF Si/SILICIDE/Si STRUCTURES

A. Introduction

Epitaxial Si/silicide/Si structures have been grown using MBE[3,45,46] and non-UHV techniques,[47] with relatively thick silicide layers ($\sim$1000 Å). The best results have been achieved with $CoSi_2$ and $NiSi_2$ layers on Si(111). Processing in UHV generally yields results far superior to those from non-UHV techniques. Si growth on the surface of a bulk silicide crystal has also been reported.[48] The growth of Si/silicide/Si structures on substrates with orientation other than (111) has proved to be difficult,[45] and no satisfactory results have yet been reported in the literature.

The unusual uniformity and smoothness of very thin ($<$100 Å) epitaxial silicide layers naturally suggests the utilization of such layers as the buried metal in a semiconductor/metal/semiconductor structure constituting a metal base transistor (MBT).[49] The advantages of epitaxial silicide over other materials are the possibility of fabricating single crystal metallic layers with perfect interfaces with the semiconductors and the fact that the thickness of the uniform metallic layers may be made such that it is comparable to or less than an electron mean free path in the metallic compound. Beside the technological impact stemming from the high speed expected of such a device, a metal base transistor also offers a unique opportunity to study hot electron transport in metals and understand quantum mechanical mechanisms at the metal semiconductor interface. Superlattices comprised of ultrathin epitaxial silicide and silicon layers are a new class of materials made possible by the development of epitaxial silicide technology with potentially important optical and electronic properties. With all these motivations, it is not surprising that recently a great deal of effort has gone into the growth of epitaxial silicon layers on thin epitaxial silicide layers.

B. Growth of Si/$NiSi_2$/Si structures

Earlier attempts to grow Si/$NiSi_2$/Si structures[45] have been hampered by the instability of $NiSi_2$ which tends to diffuse to the surface as Si is deposited. For thick $NiSi_2$ layers ($\sim$1000 Å) with misfit dislocations at the interface, this problem seemed to be averted.[50] However, for interesting applications such as the MBT, a silicide thickness of less than $\sim$100 Å is desired. The growth of uniform, strained heterostructures of such thin layers represents a more difficult task. It was discovered that when a few thousand Å of Si is deposited at $\sim$500–600 °C on the surface of thin $NiSi_2$ layers, an uneven surface is seen afterward on which Ni can be detected by AES (see Fig. 9). RBS analysis showed that the $NiSi_2$ layer became discontinuous and broadened to the surface.

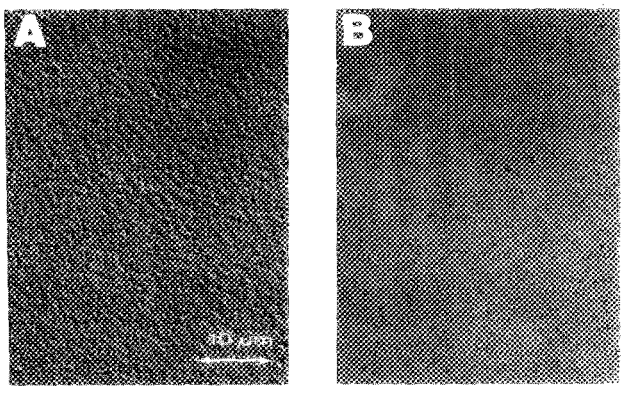

FIG. 9. Nomarski micrographs of the surface of heteroepitaxial Si(111)/65 Å $NiSi_2$/1500 Å Si structures grown at ~520 °C. (a) No Si template was used (b) a 20 Å Si template was grown before the Si MBE growth.

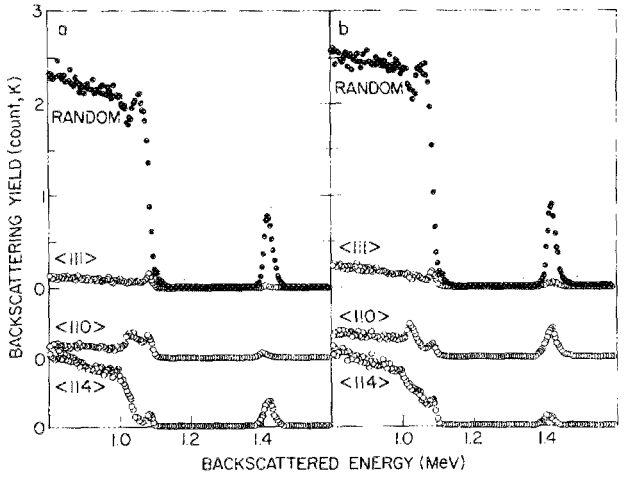

FIG. 10. Channeling and random RBS spectra of epitaxial Si(111)/90 Å $NiSi_2$/1500 Å Si structures. (a) Of the A/A/B orientation; (b) of the A/B/A orientation.

This problem may be remedied by the use of a silicon template layer.[51] After a thin $NiSi_2$ layer is first grown on Si(111) by the method described in Sec. II A, a thin (~10–30 Å) Si layer is deposited on the surface of the silicide at room temperature. A short anneal at ~400–500 °C allows the epitaxial ordering of the deposited Si layer, and a sharp 7×7 LEED pattern appears after annealing. The Ni to Si ratio of AES is unchanged before and after the anneal, indicating little diffusion has taken place. The intensity of the integral LEED beams is much larger than the reconstructed beams. For Si thickness of ~15–30 Å, the integer spots show strong threefold symmetry; the pattern, however, is similar to the original $NiSi_2$ pattern with a 180° rotation. Because a shift in intensity between (1, 0) and (0, 1) type beams usually comes from a change in the position of the second atomic layer relative to the surface Si layer, the observation of a rotated pattern suggests that the Si layer was rotated by 180° with respect to the $NiSi_2$. TEM shows that although the Si template layer is somewhat rough, it appears to cover the majority of the $NiSi_2$ surface.[51]

The template method is very effective for Si growth on silicide. With the presence of this Si template, the surface becomes smooth and impurity free under the same Si growth conditions, as shown in Fig. 9(b). RBS and channeling spectra of typical heterostructures grown with the use of a Si template are shown in Fig. 10. The buried $NiSi_2$ layers remain uniform. A χ_{min} of ~3% is measured for the Si overlayers, indicating the near-perfect crystallinity of the epitaxial structure. Channeling along the inclined ⟨110⟩ and ⟨114⟩ axes shows that the top Si layer occupies the same orientation as the original Si template, namely rotated 180° with respect to $NiSi_2$. Taking advantage of the $NiSi_2$ template technique,[8] we have been able to grow strained epitaxial $Si_{sub}/NiSi_2/Si_{over}$ structures with A/B/A and A/A/B orientations.[51] TEM analysis shows these structures to be uniform and essentially pseudomorphic. Pinhole density is negligibly small compared with that in thin $CoSi_2$ layers.

Good quality heterostructures on Si(100) have proved more difficult to fabricate. The MBE growth temperature for Si on $NiSi_2$(100) is lower than with (111). Using a Si template, good quality Si layers (χ_{min} = 6%) may be grown at 400–470 °C.[51] No nickel was found on the surface after Si deposition. However, TEM studies of such samples in cross section reveal that the interface between $NiSi_2$ and Si overlayer has become faceted along {111} planes. There are also pinholes in the $NiSi_2$ layer allowing the Si overlayer to be connected with the substrate Si. However, the likelihood of improving (100) heterostructures by the use of suitable template layers has not yet been fully explored.

C. Growth of Si/$CoSi_2$/Si structures

Studies of the electron transport in epitaxial $CoSi_2$ thin films have revealed a long mean free path for conduction electrons close to the Fermi energy in this metal.[52] There is also evidence for specular scattering off the boundaries, suggesting an extraordinary coherency of the silicide–Si interface.[53] These, and other observations, establish thin $CoSi_2$ layers as a candidate for possible application as the base material in a metal base transistor. With this in mind, the formation of ultrathin (100 Å) $CoSi_2$ layers has been investigated recently. As this is a fast moving field with a strong device overtone, publication has lagged behind actual research progress. From the standpoint of high speed device applications, epitaxial structures of Si/$CoSi_2$/Si are more attractive than similar structures consisting of $NiSi_2$. This is because of the excellent conductivity of cobalt disilicide and the long electron mean free path.[52] However, due to the large lattice mismatch with Si, perfect epitaxial double $CoSi_2$ heterostructures are difficult to fabricate. Unlike $NiSi_2$, the growth of such heterostructures does not suffer from the instability of thin silicide layers during subsequent Si epitaxial growth. Rather, the problem rests with the pinholes that are always present in the silicide layers. Although excellent quality epitaxial double heterostructures may be grown, as evidenced by their excellent channeling behavior, detailed TEM analyses indicate that a low density of small pinholes still exists, the effect of which on electron transport cannot be neglected.

Epitaxial growth of Si on thin layers of $CoSi_2$ is greatly influenced by the use of thin (~20 Å) Si templates prior to thick (>1000Å) Si evaporations. These template layers

were grown by deposition at room temperature on the silicide and annealing to ~600 °C for ~1 min. The best quality Si layers, as judged by the measured channeling χ_{min}'s, are grown at ~600–650 °C with a suitable Si template. Sharp 7×7 LEED patterns are observed after such a deposition, and no impurities are found on the surface by AES analysis.[24] Overgrown Si layers contained a low density of misfit dislocations at the $CoSi_2$/Si interface and a small number of stacking fault tetrahedra. Nevertheless, the overall quality of the Si overlayers is good, as measured by ion channeling, with a χ_{min} of $\leqslant 4\%$.

Under different growth conditions, the orientation of the Si overlayer can be made pure A or B. We have found that type A Si (with respect to the Si substrate) may be grown on perforated $CoSi_2$ layers which contain a substantial fraction of type A $CoSi_2$ grains. Type B Si grows with the use of a Si template on very uniform $CoSi_2$ of pure B orientation. In general, the Si orientation depends on the orientation of the silicide, the pinhole dimension, the Si template, and the Si substrate wafer miscut. RBS spectra demonstrating these results and the high quality of overgrown silicon are shown in Fig. 11. It seems reasonable to assume that type A Si grows on type A $CoSi_2$ and on Si through the openings. Type B Si forms on the surface of type B $CoSi_2$.

V. ELECTRON TRANSPORT THROUGH Si/SILICIDE/Si STRUCTURES

Electrical characteristics of epitaxial Si/silicide/Si structures may be studied if suitable electrical contacts are made to the doped Si. Since the morphology of thin $CoSi_2$ layers may vary significantly with growth conditions, epitaxial Si/$CoSi_2$/Si heterostructures may be fabricated with a controlled distribution of pinhole characteristics. These heterostructures may then be processed into two-level mesas, with the top Si acting as the emitter, silicide layer as the base, and the Si substrate as collector. Devices fabricated from these heterostructures have been described by us in previous publications.[24,54] In Fig. 12 we show common base and common emitter current–voltage characteristics for two typical n-type samples, one with a common base current gain $\alpha \sim 0.12$ and another with $\alpha \sim 0.6$. We have observed a strong correlation between α and the size and density of pinholes, as revealed by TEM, in all the devices we have tested. This evidence suggests that electron transport through the base occurs through pinholes so that the transistor action is of a permeable base nature,[55] i.e., charge transport occurs through pinholes in the $CoSi_2$ metal base. The largest α observed for almost pinhole-free silicide was ~0.01, setting an upper limit on the magnitude of hot or "ballistic" electron transport through the metal base.

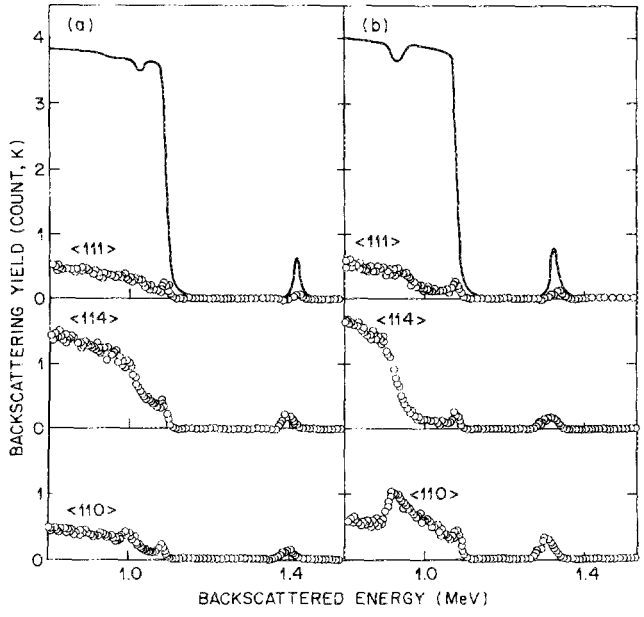

FIG. 11. Channeling and random RBS spectra from Si/$CoSi_2$/Si(111) structures. (a) A type A Si overlayer grown on mixed A + B $CoSi_2$ and (b) an essentially ABB heterostructure.

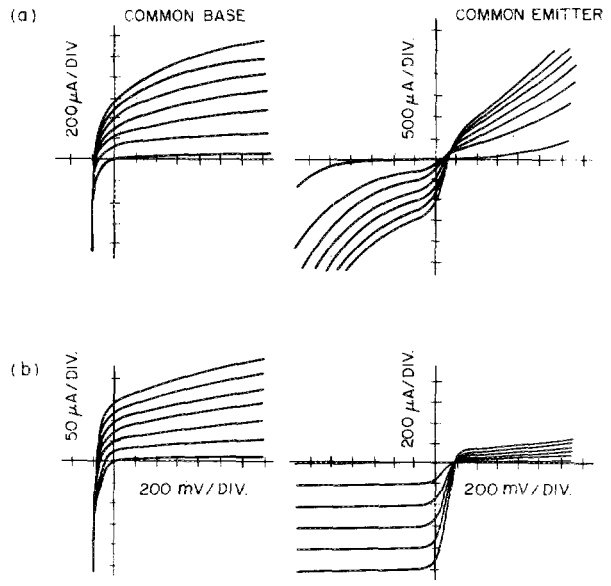

FIG. 12. Device current–voltage characteristics in the common base and common emitter configuration for a sample with $\alpha \sim 0.6$ shown in (a) and $\alpha \sim 0.12$ shown in (b). Curves were taken in steps of 200 μA beginning with $I_{cc} = 0$.

While there is little doubt that the presence of pinholes in $CoSi_2$ layers play a dominant role in electron transport across Si/$CoSi_2$/Si heterostructures, the role of ballistic transport across the metal base is still unresolved. There have been other reports which attribute the observed transistor action to the transport of hot or ballistic electrons across the metal base.[29,28,56] However, in these reports, the absence of any direct evidence for pinhole-free $CoSi_2$ layers means that such speculations are supported only indirectly through analyses of electrical characteristics.[29] In our view, a detailed understanding of the structure of thin silicide/silicon layers and the quantum mechanical processes at the silicide/silicon interface are prerequisite for a reliable interpretation of the transport mechanisms giving rise to the electrical data.

VI. CONCLUSIONS

Recent development of epitaxial silicide growth techniques has led to the formation of structurally perfect metal

semiconductor junctions. Novel behavior in the epitaxial growths has been observed and utilized to achieve single crystal epitaxy. High quality multilevel silicide–silicon epitaxial structures with very small layer thickness have been demonstrated. These and other structures represent a new materials system with exciting prospects for high speed device application and three-dimensional integration. Already, new properties of single crystal silicide–silicon interfaces have been revealed which improve our understanding of various phenomena occurring at metal–semiconductor junctions. Silicon/silicide crystal growth is a young and rapidly expanding area of research. With the versatility of modern MBE machines, new structures and new properties are only now beginning to become available. This is a very exciting time in silicide research. There are new areas with potentially interesting science and useful technology yet to be explored.

ACKNOWLEDGMENTS

We are indebted to J. M. Poate, J. C. Bean, S. Nakahara, K. K. Ng, F. C. Unterwald, M. Anzlowar, M. L. McDonald, J. Batstone, and D. C. Jacobson for their contributions to this project.

[1]K. N. Tu and J. W. Mayer, in *Thin Films Interdiffusion and Reactions*, edited by J. M. Poate, K. N. Tu, and J. W. Mayer (Wiley, New York, 1978).
[2]H. Ishiwara, Electrochem. Soc. Symp. Proc. **80-2**, 159 (1980).
[3]R. T. Tung, J. M. Poate, J. C. Bean, J. M. Gibson, and D. C. Jacobson, Thin Solid Films **93**, 77 (1982).
[4]L. J. Chen, H. C. Cheng, and W. T. Lin, Mater. Res. Soc. Symp. Proc. **54**, 245 (1986).
[5]J. M. Gibson, R. T. Tung, and J. M. Poate, Mater. Res. Soc. Symp. Proc. **14**, 395 (1983).
[6]L. J. Brillson, Surf. Sci. Rep. **2**, 123 (1982).
[7]R. T. Tung, Phys. Rev. Lett. **52**, 461 (1984).
[8]R. T. Tung, J. M. Gibson, and J. M. Poate, Phys. Rev. Lett. **50**, 429 (1983).
[9]R. T. Tung, in *Silicon Molecular Beam Epitaxy*, edited by E. Kasper and J. C. Bean (Chemical Rubber, Boca Raton, FL, 1986).
[10]P. J. Grunthaner, F. J. Grunthaner, and J. W. Mayer, J. Vac. Sci. Technol. **17**, 924 (1980).
[11]F. Comin, J. E. Rowe, and P. H. Citrin, Phys. Rev. Lett. **51**, 2402 (1983).
[12]E. J. van Loenen, J. W. M. Frenken, and J. F. Van der Veen, Appl. Phys. Lett. **45**, 41 (1984).
[13]R. T. Tung, J. M. Gibson, and J. M. Poate, Mater. Res. Soc. Symp. Proc. **14**, 435 (1983).
[14]W. S. Yang, F. Jona, and P. M. Marcus, Phys. Rev. B **28**, 7377 (1983).
[15]R. T. Tung (to be published).
[16]R. T. Tung, K. K. Ng, J. M. Gibson, and A. F. J. Levi, Phys. Rev. B **33**, 7077 (1986).
[17]R. T. Tung, J. M. Gibson, and J. M. Poate, Appl. Phys. Lett. **42**, 888 (1983).
[18]N. W. Cheung and J. W. Mayer, Phys. Rev. Lett. **46**, 671 (1981).
[19]K. C. R. Chiu, J. M. Poate, J. E. Rowe, T. T. Sheng, and A. G. Cullis, Appl. Phys. Lett. **38**, 988 (1981).
[20]Y.-J. Chang and J. L. Erskine, Phys. Rev. B **26**, 4766 (1982).
[21]R. T. Tung, S. Nakahara, and T. Boone, Appl. Phys. Lett. **46**, 895 (1985).
[22]J. M. Gibson, J. C. Bean, J. M. Poate, and R. T. Tung, Thin Solid Films **93**, 99 (1982).
[23]C. Pirri, J. C. Peruchetti, G. Gewinner, and J. Darrien, Phys. Rev. B **29**, 3391 (1984).
[24]R. T. Tung, A. F. J. Levi, and J. M. Gibson, Appl. Phys. Lett. **48**, 635 (1986).
[25]K. Ishibashi and S. Furukawa, Appl. Phys. Lett. **43**, 660 (1983).
[26]Y. C. Kao, M. Tejwani, Y. H. Xie, T. L. Lin, and K. L. Wang, J. Vac. Sci. Technol. B **3**, 596 (1985).
[27]B. D. Hunt, N. Lewis, E. L. Hall, L. G. Turner, L. J. Schowalter, M. Okamoto, and S. Hashimoto, Mater. Res. Soc. Symp. Proc. **56**, 151 (1986).
[28]C. D'Anterroches and F. Arnaud D'Avitaya, Thin Solid Films **137**, 351 (1986).
[29]E. Rosencher, S. Delage, F. Arnaud D'Avitaya, C. D'Anterroches, K. Belhaddad, and J. C. Pfister, Physica B **134**, 106 (1985).
[30]F. Arnaud D'Avitaya, S. Delage, E. Rosencher, and J. Derrien, J. Vac. Sci. Technol. B **3**, 770 (1985).
[31]D. Cherns, G. R. Anstis, J. L. Hutchison, and J. C. H. Spence, Philos. Mag. A **46**, 849 (1982).
[32]J. M. Gibson, J. C. Bean, J. M. Poate, and R. T. Tung, Appl. Phys. Lett. **41**, 818 (1982).
[33]J. M. Treacy and J. M. Gibson, J. Vac. Sci. Technol. B **4**, 1458 (1986).
[34]D. Cherns, C. J. D. Hetherington, and C. J. Humphreys, Philos. Mag. A **49**, 165 (1984).
[35]J. M. Gibson, Ultramicroscopy **14**, 1 (1984).
[36]E. J. van Loenen, J. W. M. Frenken, J. F. van der Veen, and S. Valeri, Phys. Rev. Lett. **54**, 827 (1985).
[37]R. T. Tung and J. M. Gibson, J. Vac. Sci. Technol. A **3**, 987 (1985).
[38]A. F. J. Levi, R. T. Tung, J. L. Batstone, and M. Anzlowar (to be published).
[39]Y. C. Kao, Y. Y. Wu, and K. L. Wang, Electrochem. Soc. Symp. Proc. **85-7**, 261 (1985).
[40]E. Rosencher, S. Delage, and F. Arnaud D'Avitaya, J. Vac. Sci. Technol. B **3**, 762 (1985).
[41]M. Lichr, P. E. Schmidt, F. K. LeGoues, and P. S. Ho, Phys. Rev. Lett. **54**, 2139 (1985).
[42]L. N. Aleksandrov, R. N. Lovyagin, P. A. Simonov, and I. S. Bzinkovskaya, Phys. Status Solidi A **45**, 521 (1978), and references therein.
[43]R. J. Hauenstein, T. E. Schlesinger, T. C. McGill, B. D. Hunt, and L. J. Schowalter, Appl. Phys. Lett. **47**, 853 (1985).
[44]B. D. Hunt, L. J. Schowalter, N. Lewis, E. L. Hall, R. J. Hauenstein, T. E. Schlesinger, T. C. McGill, M. Okamoto, and S. Hashimoto, Mater. Res. Soc. Symp. Proc. **54**, 479 (1986).
[45]J. C. Bean and J. M. Poate, Appl. Phys. Lett. **37**, 643 (1980).
[46]A. Ishizaka and Y. Shiraki, Jpn. J. Appl. Phys. **23**, L499 (1984).
[47]S. Saitoh, H. Ishiwara, and S. Furukawa, Appl. Phys. Lett. **37**, 203 (1980).
[48]B. D. Ditchek, J. P. Salerno, and J. V. Gormley, Appl. Phys. Lett. **47**, 1200 (1985).
[49]C. R. Crowell and S. M. Sze, Phys. Rev. Lett. **15**, 659 (1965).
[50]A. Ishizaka, P. A. Cullen, and Y. Shiraki, in Extended Abstracts of the 16th International Conference on Solid State Devices and Materials, Kobe (1984), p. 39.
[51]R. T. Tung, J. M. Gibson, and A. F. J. Levi, Appl. Phys. Lett. **48**, 1264 (1986).
[52]J. C. Hensel, R. T. Tung, J. M. Poate, and F. C. Unterwald, Appl. Phys. Lett. **44**, 913 (1984).
[53]J. C. Hensel, R. T. Tung, J. M. Poate, and F. C. Unterwald, Phys. Rev. Lett. **54**, 1840 (1985).
[54]J. C. Hensel, A. F. J. Levi, R. T. Tung, and J. M. Gibson, Appl. Phys. Lett. **47**, 151 (1985).
[55]C. O. Bozler and G. D. Alley, IEEE Trans. Electron. Devices **ED-27**, 1128 (1980).
[56]E. Rosencher, S. Delage, Y. Campidelli, and F. Arnaud D'Avitaya, Electron. Lett. **20**, 762 (1984).