8 Gbps CMOS interface for parallel fiber-optic interconnects

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Abstract

We demonstrate an 8 Gbps CMOS link interface designed for use with parallel fiber-optic interconnect technology. The link interface is implemented in 0.8 µm CMOS and consists of eight data and one frame control channel each operating at 1 Gbps along with a full-speed 1 GHz clock channel. The chip also provides dual-ported FIFO buffers for interface to a host computer.

INTRODUCTION

Parallel electrical interfaces such as SCI [1] and HIPPI-6400 [2] will be replaced by very low-cost high-bandwidth parallel fiber-optic interconnects. These fiber-optic solutions will increasingly be inserted intohigh-performance digital systems. Typically, a parallel fiber-optic port consists of 8 channels each signaling at the rate of 1 Gbps and capable of synchronous transmission over several hundred meters of ribbon fiber. While such high-density high-bandwidth interconnect technology is attractive for insertion into advanced systems, there is a mismatch between the high signaling rates of low-cost optoelectronic components such as Vertical Cavity Surface Emitting Lasers (VCSELs) and that which is achievable with conventional CMOS circuitry. Future system integration of parallel fiber-optic interconnects requires that a cost-effective bridge be established between these two technologies. Hence an important challenge is to leverage low-cost, high integration CMOS technology and directly interface to parallel fiber-optic transceiver modules. In this letter we present our initial experimental results which prove 8 Gbps data transfer rates over a byte-wide parallel interface may be achieved using 0.8 μm CMOS technology.

PRINCIPLE

Our strategy provides for a low-speed 250 MHz, 32-bit wide data path bridge from on-chip synchronous FIFO buffers to a high-speed 8 Gbps byte-wide positive referenced ECL (PECL) optoelectronic interface. The optoelectronic interface is the HP-POLO [3] module which consists of eight data, one control and one clock channel for an aggregate port signalling rate of 10 Gbps and a transceiver bisection bandwidth of 20 Gbps.

Fig. 1 shows a schematic of the link interface chip. This chip integrates an 8 Gbps transmit (Tx) and 8 Gbps receive (Rx) interface along with two dual-ported one kilobyte FIFO buffers for a host computer interface. The host computer communicates with the FIFOs at clock frequencies compatible with computer system bus clock rates (e.g. 30 MHz - 60 MHz) depending upon the system configuration. The host can write a packet into the Tx FIFO and delimits the packet with an End-Of-Packet (EOP) signal. This signal informs the controller to burst the packet out of the FIFO to the transmit portion of the chip.

The Tx portion of the high-speed 8 Gbps interface, shown on the right of Fig. 1, consists of nine

4:1 serializer and transmit driver channels. Eight of the channels are dedicated for data while one channel is used for frame control at the physical link interface. Each of the serializers are clocked by a 1 GHz system clock. This system clock is distributed on-chip over a 4 mm wide interface using a novel low-swing clock distribution scheme [4]. The clock is then locally regenerated for full-, half- and quarter-speed clocking of the serializer and further distribution of a 250 MHz clock to the Tx FIFO unit. Data is transmitted over the 8 Gbps physical layer interface along with a full-speed clock and frame control signal. At the Rx interface, shown in the left portion of Fig. 1, the clock is again distributed on-chip in a similar low-swing manner as the transmit interface. Nine 1:4 deserializer channels then produce the 32-bit data and 4-bit control signals.

An alignment unit uses the deserialized frame control signal to correct for any data misalignment between the transmit and receive interfaces of the link. Data misalignment can occur because each end-point of a link is reset independently and so the serializer and deserializer may be out of phase. The alignment unit compensates for this difference and the resulting normalized data and control signals that come out of the alignment unit are then written into the Rx FIFO to be read out later by the host computer.

For both the Tx and Rx portions of the link interface, full-speed 1 GHz processing of data require differential amplifier buffers, level shifters and master-slave latches. At 500 MHz and 250 MHz clock frequencies single-ended dynamic logic circuits are used to implement the slow speed portions of the serializer and deserializer along with the alignment unit and FIFO controllers. The memory cell of the dual-ported SRAM FIFO is a standard 8 transistor, cross-coupled inverter circuit topology. Voltage controlled sense amplifiers are used for high-speed bit-line reading.

A photograph of the fabricated die indicating the layout of the link interface circuitry is shown in Fig. 2. The die measures 10 mm x 5 mm. The FIFOs measure 3 mm x 2 mm while the high-speed serializer and deserializer interfaces both measure 4 mm x 2.5 mm. The die is housed in a ceramic quad flat package with controlled signal impedance lines. The package has -3dB bandwidth of 3 GHz and also provides two separate power planes needed for isolation of digital and analog power supplies.

Fig. 3 shows results of measurements obtained from transmitting data over the high-speed 8 Gbps interface. The left panel of the figure is an eye diagram of a single data channel operating at 1 Gbps. The panel on the right of the figure shows the seven least significant data signals along with the frame control channel during transmission of a packet containing a binary test pattern. This result was obtained using a 1 GHz clock and a sampling oscilloscope configured to its maximum of eight sampling heads. Operating the interface chip with a 1 GHz clock requires 6.2 Volts and consumes 3.2 Amps (i.e. 20 Watts). When tested using a 622 MHz clock the power supply voltage may be reduced to 4.3 Volts and the device draws 1.8 Amps (i.e. 8 Watts). All the data and control signals on the printed circuit board are deskewed to within 60 ps across the entire Tx interface port. This corresponds to 40 ps of skew for the serializer Tx interface and package along with 20 ps skew from the printed circuit board layout.

CONCLUSIONS

We have presented a new high-speed byte-wide CMOS interface optimized for direct connection to emerging parallel fiber-optic interconnect modules. Measurements prove that an 8 Gbps port is achievable in 0.8 µm CMOS with each signal line operating at 1 Gbps. The demonstration circuitry is integrated with one kilobyte FIFO buffers to facilitate future computer system insertion.

ACKNOWLEDGEMENT

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REFERENCES

[1] 'IEEE Standard for Scalable Coherent Interface (SCI)', *The Institute of Electrical and Electronics Engineers, Inc*., New York, IEEE Std 1596-1992, 1992.

[2] 'High-Performance Parallel Interface - 6400 Mbit/s Physical Layer (HIPPI-6400-PH)', *Technical Committee of Accredited Standards*, X3T11, May 1996.

[3] HAHN, K.: 'Gigabyte/s Data Communications with POLO Parallel Optical Link', *The 46th Electronics Components and Technology Conference*, Orlando, Florida, May 28-31, 1996, pp. 301-307 (IEEE cat# 96CH35931).

[4] MADHAVAN, B., SANO, B., LEVI, A. F. J.: 'A Novel High Speed Low Skew Clock Distribution Scheme in 0.8 Micron CMOS', *IEEE International Symposium on Circuits and Systems*, Atlanta, Georgia, May 12-15, 1996, Vol. 4, pp. 149-152. (IEEE cat #96CH35876, ISBN 0-7803-3073-0).

FIGURE CAPTIONS

Figure 1: Schematic of the 8 Gbps link interface circuit. The chip consists of a high-speed byte-wide transceiver interface for direct connection to a parallel optical link module (POLO). The chip also includes FIFO packet buffers for interface to a host computer.

Figure 2: Photograph of fabricated link interface die. The figure highlights the Tx FIFO, serializers, deserializers, alignment unit and Rx FIFO. The slow speed host computer TTL pads are located on the top of the chip while the one Gbps PECL pads are located at the bottom. The die measures 10 mm x 5 mm and is implemented in 0.8 μm CMOS technology.

Figure 3: Measurements of the link interface chip. The left panel shows an eye diagram for one differential data channel (D0) operating at 1 Gbps. The measured bit error rate (BER) for a non-return to zero (NRZ) pseudo-random bit stream (PRBS) of 2^{32}-1 is less than 10^{-13}. The right panel shows the positive rail of seven data channels (D0-6) and the frame control channel (FC) during the transmission of a data packet while the frame control line is high. Signals are attenuated by -20 dB so that the vertical scale for the left panel is 200 mV/div and 2 V/div for the right panel.

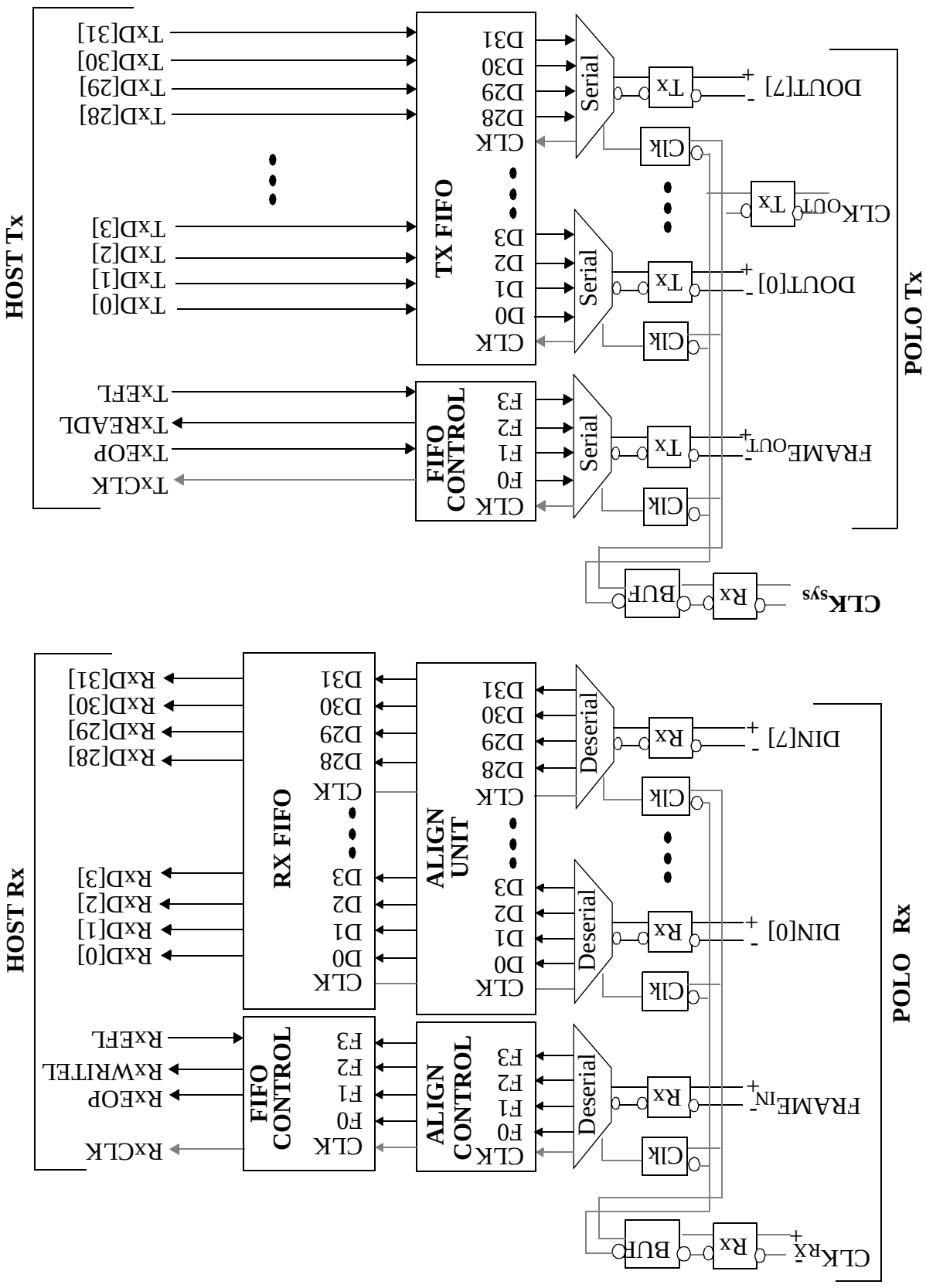

FIGURE 1. B. Sano et al. "8 Gbps CMOS interface for parallel fiber- optic interconnects"

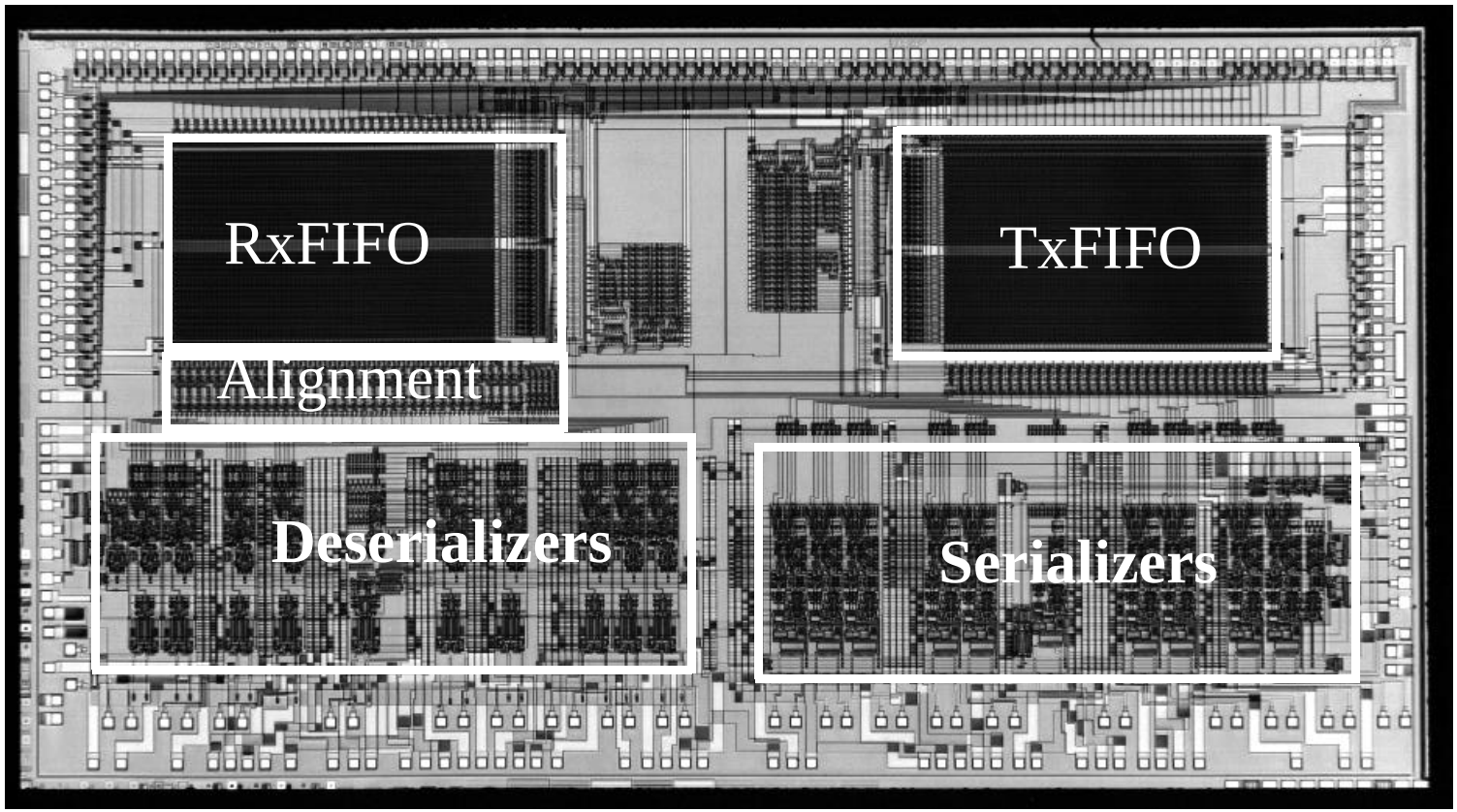

FIGURE 2. B. Sano et al. "8 Gbps CMOS interface for parallel fiber- optic interconnects"

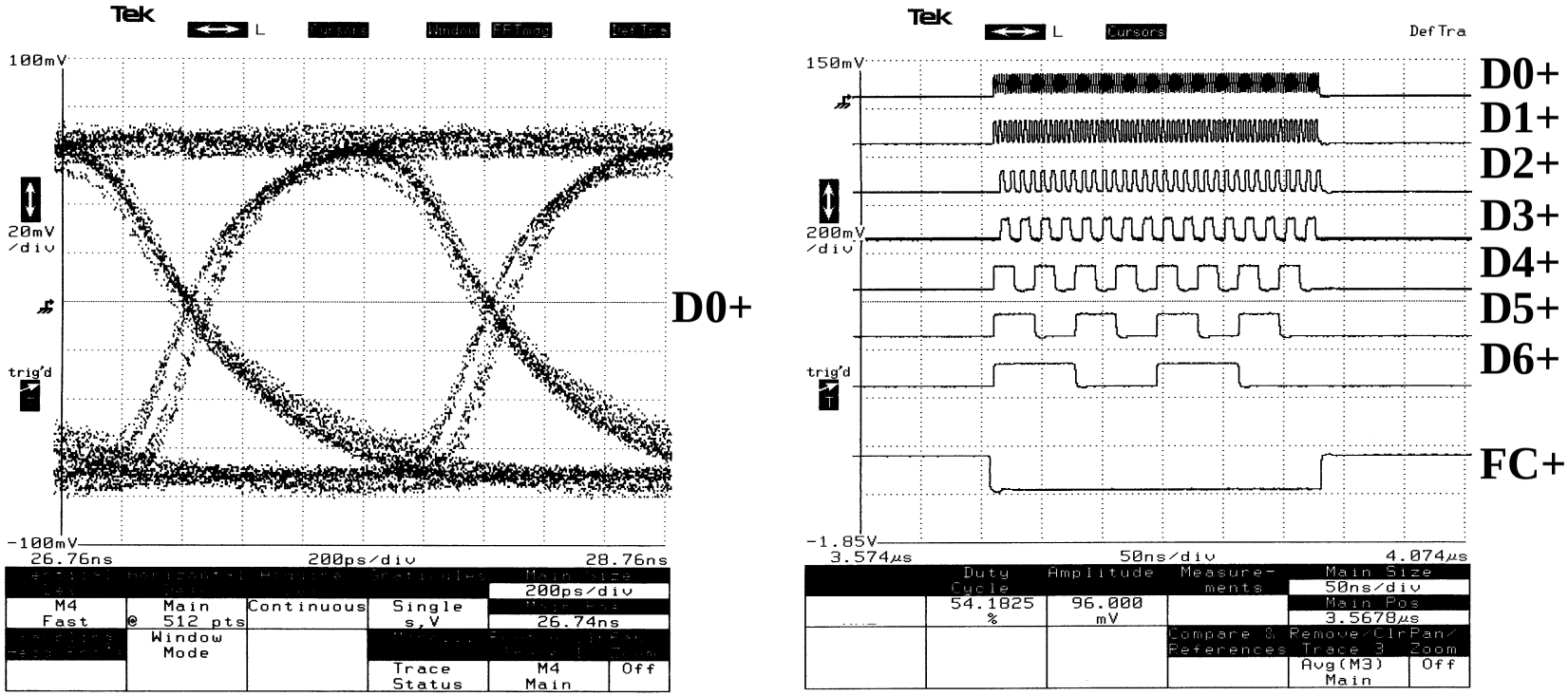

FIGURE 3. B. Sano et al. "8 Gbps CMOS interface for parallel fiber-optic interconnects"