High Performance Optical Datalink Array Technology

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***Abstract*— Demands for increased interconnection density and higher bandwidth, coupled with stringent cost constraints of advanced wide bandwidth telecommunication switching and high throughput computer architectures, are exhausting conventional electrical interconnection capabilities. The requirement for greater interconnection capabilities, spawned in part by the advances in integrated circuit technologies and the need for enhanced digital services, dictate that technology advancement must occur in traditional electronic packaging and/or interconnection techniques. The resolution of these technological needs is paramount for the successful competitive introduction of these systems. Presently, a "bottleneck" occurs at the board-to-board level of the interconnection hierarchy. Therefore, an opportunity exists for the development of new *parallel optical* interconnection techniques which can be incorporated into system designs beginning at this interconnection level and beyond. The strategic insertion of parallel optical interconnection technology into these electronic processing systems not only meets projected performance requirements, but potentially offers them at a competitive cost.**

I. Introduction

IT has been known for some time that high performance computing and switching systems can benefit from the use of cost effective optical interconnection over length scales greater than approximately 1 m [1]. In order to fulfill the needs of many small volume users, which in aggregate create a very large demand for parallel optical modules, these optical modules should conform to an industry standard so that they can be applied to different applications without customization. The IEEE Std. 1596-1992 Scalable Coherent Interface (SCI) provides such a standard. It supplies computer bus-like services but uses a collection of fast point-to-point links (of size $16N + 2$) instead of a physical bus in order to reach higher data rates (i.e., 1 Gb/s per link). This standard provides a framework for developing parallel optical technologies such as the one-dimensional optical data link (1D-ODL) proposed in this paper.

The key technological developments necessary for the implementation of the 1D-ODL are: laser diode arrays; detector diode arrays; solder bump bonding; electronic laser driver arrays; electronic receiver arrays; optical submount technologies (e.g., micromachined silicon with waveguide capability); optical fiber ribbon cables; and optical fiber connectorization. Fig. 1 shows a technology schematic for the implementation of AT&T's 1D-ODL. These key technologies allow the following system design advantages: low cost optical data links (package and manufacturing cost are shared over many channels); high bandwidth; high reliability; ruggedized piece parts for manufacturing environments; high optical interconnection density; low skew (useful for synchronous designs); small module footprint ($\sim 6.5\,\text{cm}^2$); and low EMI. This represents a significant cost/performance advantage over an alternative serial ODL scheme (which makes use of discrete devices), or an all electronic interconnection scheme. In this paper we report our initial implementation of a 1D-ODL.

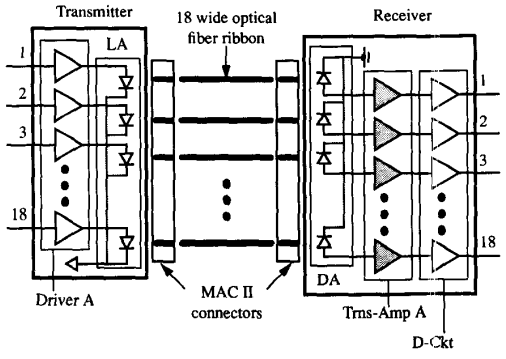

Fig. 1. 1D-ODL technology schematic diagram.

Critical to the development of the 1D-ODL program is the adoption of appropriate packaging. The transmitter and receiver modules must be compatible with an existing fiber ribbon connector. One such fiber ribbon connector, is AT&T's Multi-fiber Array Connector (MAC-II), which consists of 12 or 18 wide multimode (or single-mode) glass fibers placed in accurately machined silicon v-grooves on 250-μm centers. Guide pins ensure that the polished ends of the two connector halves can be accurately butt-coupled together with minimal ($\sim$ 0.5 dB for a multimode connector) coupling loss. For the MAC-II, the standard deviation for fiber misalignment is less than 2 μm. Our strategy is to bond the laser array (or detector array) on a silicon submount that incorporates v-grooves and guide pin features that will be compatible to the MAC-II connector, and hence, obtain a passive alignment scheme.

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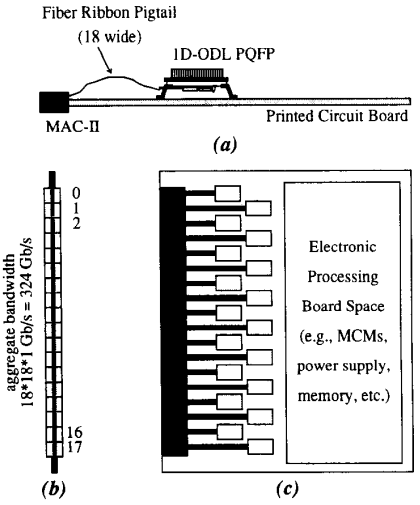

Fig. 2. System physical design application example of the 1D-ODL. (PCB (a) side view, (b) end view, and (c) top view).

AuSn solder is used to flip-chip bump bond the edge emitting laser arrays to the silicon submount. The use of AuSn solder ensures good mechanical strength, good thermal contact between the laser/submount interface, and guarantees very accurate lateral/vertical alignment. The self-alignment that occurs during solder reflow (measured to be less than 3 μm between the chip and the submount) results in a minimum of misalignment between the laser array and the fiber array. This in turn results in a high coupling efficiency across the array.

Fig. 2 diagrammatically shows how printed circuit board designers could use these 1D-ODL's. The modules can be surface mounted onto the board and then at the appropriate point in the manufacturing process, the MAC-II connectors can be mounted and connected to the 1D-ODL. The figure shows 18 1D-ODL modules mounted on a circuit board allowing an aggregate bandwidth of 324 Gb/s off the circuit board. This represents a significant improvement over "traditional" circuit board bandwidth options. The low profile nature and low power dissipation of the 1D-ODL's can allow for 1-in spacing between circuit boards in a shelf of equipment.

In summary, this paper will present the initial packaging strategy and results of a high performance 1D-ODL. Currently, development work includes cost reducing the package by use of a smaller ceramic and by utilizing a plastic injection molded housing. The housing is being designed so that it can be edge mounted on the circuit board for board-to-backplane interconnection.

II. 1D-ODL Prototype Package Design

The design and development of an appropriate packaging scheme is essential for the successful introduction of new concepts into production grade products. The authors attempted to blend components currently in production (or extensions thereof) with a minimum of technology development so that the transition to product state would be faster with less risk. The description of the package design for the 1D-ODL is partitioned into two sections. The first section describes the subassembly where the optical components are housed, and the second section describes how the optical subassembly is packaged.

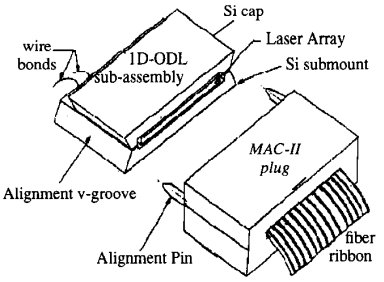

Fig. 3. 1D-ODL transmitter optical silicon subassembly to MAC II connectorization scheme.

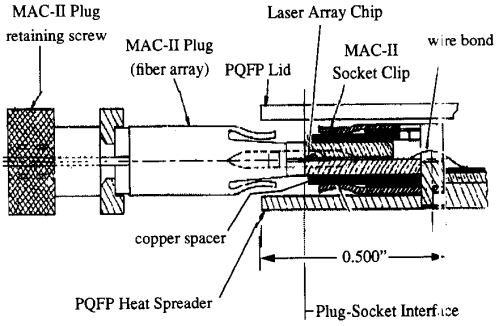

Fig. 4. 1D-ODL packaged transmitter module to MAC-II connector (cross-sectional edge view).

A. Silicon Submount Design

The goal of the 1D-ODL package design was to develop a connectorized transmitter (or receiver) module and assemble it within the tolerances needed to couple light from a laser array into a multimode fiber array using a strictly *passive* alignment scheme. Also, the module was designed to fit inside a standard 1-in square surface mountable plastic quad flat pack (PQFP). To make the design compatible with the existing ribbon connectors, AT&T's MAC-II [2], an 18 wide fiber ribbon connector was chosen. To be consistent with the fiber array connector, $\langle 100 \rangle$ silicon was used for the laser (and PiN) subassemblies. Also, silicon provides a good thermal path for heat dissipation and can be machined to lithographic accuracies [3]. Figs. 3 and 4, respectively, show the alignment methodology and the 1D-ODL transmitter module packaging scheme. The alignment between the multimode fiber array and the laser was obtained by spring loading the alignment pins in the fiber array (MAC-II plug) into the alignment v-grooves in the transmitter module. The alignment v-grooves along the edges of the transmitter module were formed by precisely etching the silicon submount and the cap. The bonding pads on the submount (corresponding to the p-contacts of the laser array) are located with respect to the etched v-grooves within lithographic accuracies.

The laser array chip consists of 18 lasers located on 250-μm centers and is bonded onto the silicon submount using Au/Sn

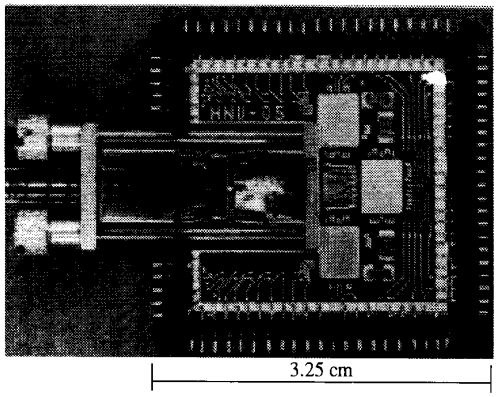

Fig. 5. 1D-ODL transmitter module photograph.

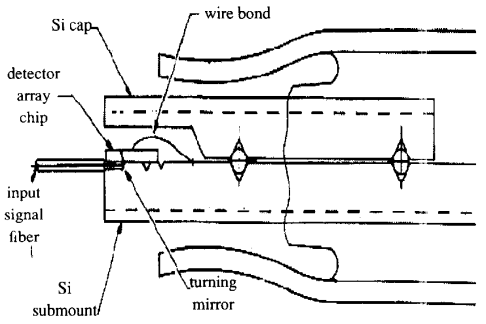

Fig. 6. 1D-ODL receiver optical subassembly (cross-sectional edge view).

solder with the epi-side towards the submount. As shown in Fig. 4, the solder bonding pads on the silicon submount are located at the end of electrical interconnection lines and are used for driving the lasers. The solder bump height was optimized to provide a good mechanical joint, to dissipate the heat generated by the lasers and to allow for the self-alignment of the laser array during the reflow process. A residue-free active atmosphere solder reflow process [4], which does not require any post-cleaning, was used to keep the laser surface void of contamination.

With the above design and assembly process, we have achieved a *passive* alignment accuracy of less than 8 μm, which is more than sufficient for applications that use multimode fibers. The misalignment that occurs includes inaccuracies in lithography, solder self-alignment, laser active area-to-bonding pad mismatch, and the connectorization scheme.

To remove the heat generated by the laser array, two copper blocks were attached to increase the thermal mass, which in turn was mounted on a Cu–Mo heat spreader. Thermal impedance of 35°C/W per laser has been measured, which is well within the range of values reported in the literature [5], [6]. The thermal crosstalk was measured and simulated, to verify its negligible effects. A photograph of the completely assembled transmitter module is shown in Fig. 5.

Fig. 6 shows the schematic of the receiver module. The packaging scheme and the silicon submount design are identical to the transmitter module except for the incorporation of gold surfaced turning mirrors in the submount, which is used to direct incoming light signals onto the PiN array. Interestingly, the shallow v-grooves etched in the receivers Si submount that directs the incident light towards the turning mirrors form a "light-pipe" which efficiently guides the light.

B. Hybrid Design

The package for the 1D-ODL is based on the AT&T developed family of multilayer hybrid integrated circuits called POLYHIC [7]. The unassembled thin film interconnect, called a POLYFIC, consists of copper-based low-loss patterned metal layers, separated by an AT&T developed triazine-based photodefinable polymer [8], on a 99.6% alumina substrate. The good dielectric properties of the polymer (relative dielectric constant, $\epsilon_r = 2.8$ and loss tangent, $\tan\delta < 0.025$), together with the ability to form low-loss controlled impedance interconnections, allows the implementation of designs at data rates that exceed 2 Gb/s [9]. Precision thin film resistors, fabricated on the ceramic substrate, are placed close to the ends of signal traces to provide excellent termination of high data rate lines.

The POLYHIC circuit is often attached to a heat spreader. For this application, a cavity has been laser milled in the alumina substrate to allow the silicon submount to be directly attached to the heat spreader. This allows optimal thermal management of the optical modules and a more compact package geometry. The active devices, in the 1D-ODL, are die and wire bonded onto the POLYFIC. Bypass capacitors are attached by reflow soldering.

The package geometry was chosen to fit one of AT&T's standard multichip module package sizes; JEDEC standard, 84 I/O with 0.050-in pitch leads (1.28 in by 1.28 in package footprint). This was done to allow the utilization of existing trim and form tools. The leadframe was implemented in a premolded form where the leadframes are molded into a plastic collar prior to attachment on the POLYHIC. Electrical leads were removed, as needed, to allow an opening in the edge of the package where the slide-on optical ribbon connector attaches to the POLYHIC. This was done to eliminate the need for a custom post-molded die cavity. The lead frame, used in previous designs, is known to support data rates > 1 Gb/s. The package is finished by RTV encapsulation and lid attachment. Fig. 5 is a photograph of the transmitter package minus RTV and lid attachment. Much of the package design was predicated by the desire to minimize development cost and interval, hence, the use of a pre-existing premolded leadframe and a quad flat pack geometry. For an initial predevelopment activity, the package configuration was optimal. From a system designers standpoint, however, a slightly different package geometry is preferred. First, it is desirable for the optical connector to be mounted to the edge of the printed wiring board such that optical connections can be accomplished "automatically" when the board is slid into the rack, similar to the way electrical connections are made. Second, a smaller edge profile, to minimize the amount of board edge occupied by the connector, would be desirable (see Fig. 7). There are current plans are to evolve the package in this direction.

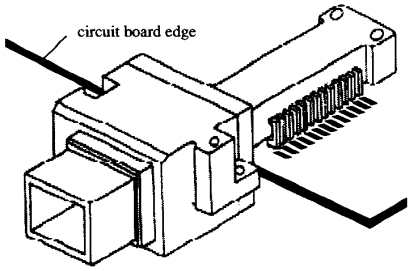

Fig. 7. 1D-ODL edge mounted package concept drawing.

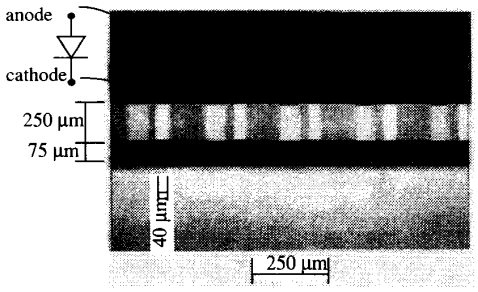

Fig. 8. InP 18 wide edge emitting laser array.

III. 1D-ODL Performance

The key performance indexes of any interconnection technology with respect to a large digital system design are: signal density (on/off of the PCB as well as the PCB footprint), signal bandwidth, interconnection length limitations, cost per interconnection, skew, signal group delay variations, bit error rate, and reliability. The discussion of the performance of the 1D-ODL is divided up into two subsections. The first subsection describes the transmitter module performance while the next subsection describes the receiver module.

A. Transmitter

The 18 wide laser diode arrays used in the 1D-ODL were N-substrate, Fabry-Perot, InGaAs/InP ($\lambda = 1.3$ μm), bulk active, with P-N junction blocking layers. A photomicrograph of an array is shown in Fig. 8. The laser facets are on 250-μm centers (to match the fiber ribbon connector) and have a cavity length of 250 μm. The -3-dB bandwidth of these lasers is greater than 2 GHz. The arrays are "high temperature" lasers, meaning that thermal electric coolers are not required. The laser's threshold current is in the 10–15-mA range with a reasonable uniformity. The lasers are capable of supplying several milliwatts of light power at 85°C. Since the lasers are "butt" coupled to the MAC-II connector, the amount of power coupled into the fiber will be reduced by no more than 3 dB. We desire approximately 1 mW of optical power "coupled" into the fiber.

The philosophy behind the transmitter module electronic design centers on a direct digital drive of the laser. This means that the electronic current driver delivers a step of current to the laser in which the magnitude of the current pulse in the "on" state is well above the lasing threshold (usually a factor of 2–10 times). This is accomplished *without*

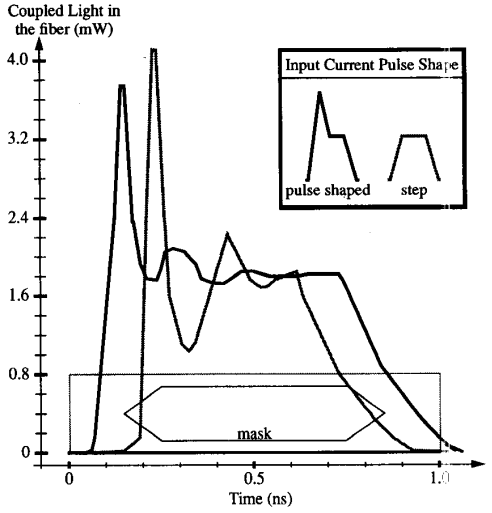

Fig. 9. Simulated transient response using a low threshold laser with various input current pulse shapes.

feedback (i.e., back facet monitors). Two design constraints immediately arise when considering this strategy. The first regards the magnitude of the current pulse. It must be large enough to deliver milliwatts of optical power in the worst-case situation (i.e., high temperature and near end of life). The second constraint concerns the current pulse shape. Since the laser is not prebiased above threshold, the turn-on delay can become excessive if the laser's threshold current is too high with respect to the current pulse height. This obstacle can be averted with proper design of the current pulse shape and proper engineering of the laser properties (e.g., coating design, cavity length, active area design, etc.). It is obviously desirable to maintain a low laser threshold current (while still maintaining high output power levels) in order to maximize signal fidelity and minimize transmitter power dissipation. Fig. 9 shows a simulated "optical eye diagram" using two different current pulse shapes to support a 1 Gb/s data rate. The lightly dashed line represents a step function current pulse (with $\tau_r = \tau_f = 250$ ps, and a 20-mA magnitude). The solid line is a shaped current pulse (with a 40-mA initial spike settling back down to the 20-mA level). Note that with pulse shaping, the relaxation oscillation peaks are smaller and the settling time is reduced. The conclusion drawn from this simulation is that direct current modulation, with pulse shaping, can result in an excellent eye diagram at 1 Gb/s in which a digital logic zero corresponds to no emitted photons.

B. Receiver

The 18 wide detector arrays used in the 1D-ODL are N-substrate, bottom illuminated, InGaAs PIN diodes. The optically active region is 75 μm in diameter on 250-μm centers. The detector arrays are mounted on top of a turning mirror (anisotropically etched on the silicon submount), so as to "up-reflect" the light from the butt-coupled MAC-II connector. The measured loss of optical power from the MAC-II to the detector array is less than 3 dB.

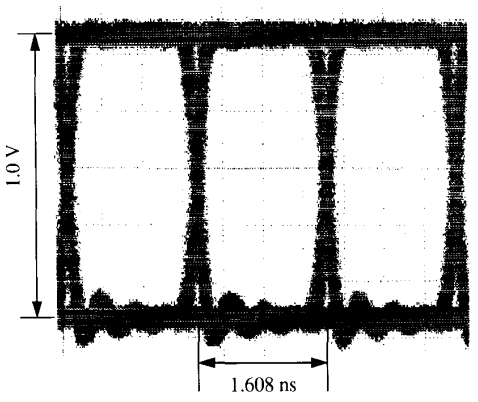

Fig. 10. Eye diagram of a pseudorandom pattern (2^{15}-1) NRZ input signal through the 1D-ODL at 622 Mb/s.

The receiver module design philosophy counters that of traditional telecommunication receiver design strategies. Here, high incident optical power on the detector array produces a large current signal to the transimpedance amplifier array IC. With such a large signal, the requirements on the transimpedance amplifier are significantly relaxed in terms of gain and dynamic range. The transimpedance gain can be relaxed, for example, to 300 Ω. This allows the integration of multiple amplifiers onto a single IC (otherwise, crosstalk limits one to discrete amplifiers). For example, assume 500 μW of light power is absorbed in the detector. At a 85% quantum efficiency, an output current of 425 μA will result. Using a transimpedance gain of 300 Ω, an output voltage of 125 mV is produced. The output of a transimpedance amplifier is generally connected to a decision circuit, where the input signal is "regenerated." The 125-mV signal in this example is quite sufficient to drive the decision circuit. In fact, we estimate a per channel power dissipation of approximately 100 mW. This results in a total power dissipation of 1.8 W on the receiver module.

Fig. 10 shows an eye diagram for a channel utilizing 1D-ODL modules. The receivers' electronics was implemented with discrete devices (Hewlett Packard transimpedance amplifiers and decision circuits). An input SONET data rate of 622 Mb/s (OC-12) was used. The pattern generator produces a pseudorandom pattern length of 2^{15}-1 of nonreturn to zero (NRZ) data. A high quality, ECL level compatible output eye was thus achieved.

IV. Conclusions

Advanced switching (and computer) system architecture designs require higher performance and lower cost packaging technologies to implement new product capabilities and enhanced services. Presently, electronic interconnection techniques (e.g., C4 and MCMs) offer superior performance at a lower cost for the chip-to-chip packaging level over that of alternative methods. Optical interconnection strategies offer advantages at higher levels of packaging (i.e., board-to-board, shelf-to-shelf, and frame-to-frame level of interconnections). Furthermore, high data rate parallel optical data links can presently offer greater flexibility and lower cost than time multiplexed serial data links.

Of the numerous techniques for implementation of a parallel data link, the 1D-ODL solution has the potential of providing, in the near term, high performance at a low cost. The key concepts offered by 1D-ODL technology that designers can take advantage of include: a dc coupled system (i.e., ECL compatible), high optical output power and contrast (vastly simplifying the receiver circuit design), improved skew, lower total power dissipation, small PCB footprint, and high temperature performance with a low thermal impedance.

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